AN INTEGRATED CIRCUIT WITH SINGLE FUNCTIONAL UNIT LEVEL INTEGRATION OF ELECTRONIC AND PHOTONIC ELEMENTS: DESIGN OF THE FET - LET HYBRID 6T SRAM AND THE ELEMENTS

by

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ABSTRACT

ANTARDIPAN PAL. An Integrated Circuit With Single Functional Unit Level Integration Of Electronic And Photonic Elements: Design Of The FET - LET Hybrid 6T SRAM And The Elements
(Under the direction of DR. YONG ZHANG)

Continuous scaling of complementary metal-oxide-semiconductor (CMOS) transistor technology over the past few decades following Moore's law has led to significant enhancement in the speed and performance of computing architectures. In today's world with high demand in data processing, CMOS scaling is focusing more on low power, cost-effective processes, and high performance to meet the requirements of high-end computations. To meet the high computation demands, reengineered, high performance, and low power device structures were necessary, and hence field effect transistors (FET) structures have evolved from planner to multi-gate, and gate all around (GAA) structures. Also, other than the very well matured silicon electronics, advanced technologies allowing heterogeneous integration of different materials systems (e.g., Si, Ge, III–V, and II-VI groups) have been developed. Though heterogeneous integration of silicon electronics with compound semiconductors can be beneficial, such developments in hybrid integration cannot address the fundamental limitations of the pure CMOS circuits, the resistive capacitive (RC) delay associated with metallic wires, and the dielectric gate delay associated with FETs. These delays ultimately limit the data speed and energy consumption.

In this research work we have explored novel applications in electronic-photonic integrated circuits of a special type of metal-semiconductor-metal (MSM) photoconductive structure known as the light effect transistor (LET) which can emulate the current voltage characteristics of a FET but with much better performances in terms of switching speed (considering carrier transit delay), energy consumption per switch and I_{on}/I_{off} ratio, and also other optoelectronic functions like optical

logic gates, optical summation, optical amplification, and optoelectronic analog operation using LETs, which cannot be done using FETs. The LET can provide extremely fast optoelectronic switching (of the order of ~ ps), and its simplistic structure does-not add unwanted parasitic and leakages which are common in all gated FETs.

To understand the superiority of LETs over FETs, particularly the potential vast performance improvement in a hybrid integrated circuit of the two types of devices, we have explored the possibilities of LETs to replace some FETs in various pure electronic circuits. Using analytical relations and simulations, we have extensively studied the effect of replacing the access FETs in a 6T SRAM (six transistor static random-access memory) structure with LETs and have made some drastic changes in the hybrid 6T FET - LET structure by replacing the whole electrical wordline with an optical waveguide (OWG). We have also proposed a prototype novel hybrid 3D integration scheme for the 6T SRAM architecture where all the typical electronic and optoelectronic components (4T FET latch, access LETs, bit lines, peripherals, etc.) will be placed on a single electronic layer while photonic components (OWGs, on-chip lasers to drive the OWGs, etc.) will be placed separately on the photonic layer with regularly spaced openings that provide the optical signal for switching four LETs grouped together from two adjacent hybrid 6T cells in the electronic layer. Also, a fully functional FET - LET hybrid SRAM bit cell with superior performance has been designed and implemented using the *mixed-mode* design environment of Synopsys Sentaurus TCAD.

DEDICATION

To my father and my uncle, in their loving memory.

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CHAPTER 1: Introduction

1.1 Motivation

Over the last decade, there has been a huge boom in CMOS photonics, and it has opened up whole new paths toward advancements in integrated circuits (ICs) and integrated systems in the post-Moore scaling era. Over the last decade, the improvements in photonic integrated circuits are mostly due to the heterogeneous integration of novel optoelectronic devices with standard CMOS circuits. Figure 1.1 [1] shows the optoelectronic signal flow in a typical electronic – photonic integrated circuit (EPIC), where the active photonic devices (for instance photodetector) can act as an optoelectronic switch and can be placed in the photodetector section such that its electrical output can drive the CMOS circuit.

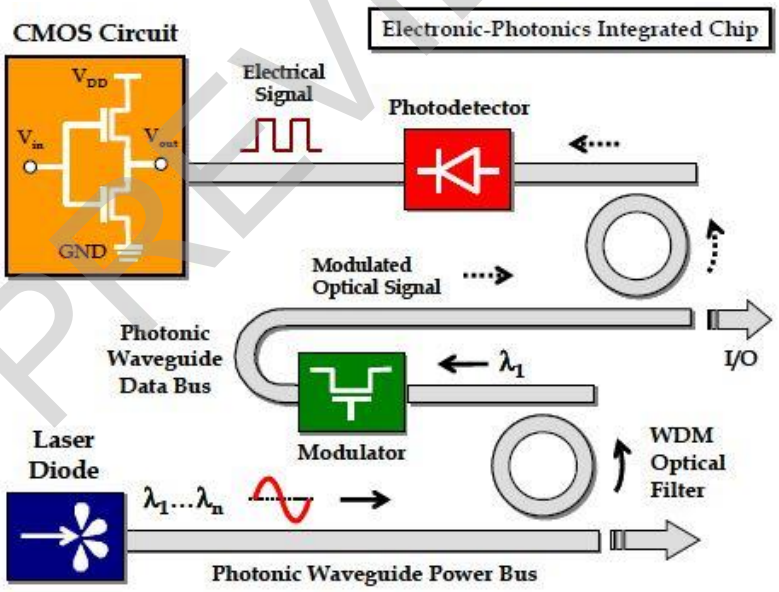

Figure 1.1: Signal flow path in an Electronic-Photonic Integrated Circuit [1]

To significantly ameliorate the energy-efficiency and data capacity of communication systems and ICs, and high preformation computing circuits, the combined use of hybrid electronic-photonic ICs have become extremely important [2-4]. The main advantage of using photons in place of electrons to process and transfer data at speeds reaching Terabits/s, over longer distances, is the much lower energy dissipation in purely photonic systems, as compared to the dissipative metal electrical wires. Among all platforms for building photonic integrated circuits (PICs), silicon on-insulator (SOI) is the most promising due to the CMOS compatible process enabled by low-cost and large-volume manufacturing. Silicon photonics integrated circuits (SiPICs) have become a potentially matured technology that can satisfy the exponentially increasing need for higher data rates with very small energy consumption, compact size, and significantly lower cost compared to discrete photonics or III-V or II-VI materials and systems [5, 6].

Some important electronic design goals are: (1) reduction of gate latency, (2) ultra-low energy consumption per bit, and (3) simplified circuit topology (for instance logic operations using optoelectronic logic circuits require a lesser number of active devices compared to all FET based CMOS circuit) and layout architecture for many complex computation structures [3]. Compared to computation, logic operation, and switching with optics, optical interconnects have been more intensively investigated due to their advantages over metal interconnects especially in intra and inter-chip communications [1]. Though over the last decade optical interconnects have been of most interest, it is also possible to have optical computations and logic operations such as implementing basic Boolean operations like the (N)AND, (N)OR, and X(N)OR logic gates and even more complex functionalities such as 1-bit half and full adders [3, 4]. Moreover, most recently,

an ultra-fast low-power deep learning network has been implemented by optical mach-mehnder interferometers (MZIs) and has consolidated the position of computation with photonics [7].

In recent times silicon photonics has been leveraging the CMOS infrastructure to address the growing demands for optical communications for internet and data center networks. The close integration of silicon photonics with CMOS promises to transform electronic–photonic technologies, enabling processor and memory chips with high-bandwidth optical input/output as discussed in [8, 9]. In the real world, photonic devices need to be integrated with a variety of nanoelectronic functions (digital, analog, memory, storage, and so on) on a single silicon die (chip). Monolithic (that is on a single chip) integration of photonic devices in close proximity to typical electronic devices like FETs is mainly crucial for reasons like allowing to achieve of high levels of performance, scalability, and complexity simultaneously for electronic–photonic systems [8, 9].

In conventional logic gates, data loss is a significant issue, and it is mainly caused since the number of inputs and outputs are not equal. It was shown by Landauer [10, 11] that the traditional Boolean logic gate for its regular operation, must dissipate energy at least kTln2 per bit loss, where k is the Boltzmann constant and T is the absolute temperature. In today's electronic systems, Ohmic loss (I^2R) is inevitable and occurs due to the flow of electrons through a conducting/semiconducting medium. Hence, in today's data centric era, an increase in power consumption is becoming a bottleneck for high performance VLSI circuits and systems. Even though CMOS technology is the most widely used in a VLSI circuit because of its low power consumption, the energy dissipated during charging and discharging operations cannot be abolished without sacrificing the circuit operation, since it is proportional to the clock frequency of the circuits [12]. On the other hand, photon being the ultimate unit of information traveling with the speed of light (with a bandwidth of THz), and with data packets of zero effective mass forming

an optical signal, the techniques of computing with light may provide a way out of the limitations of computational speed, bandwidth limitations, power dissipation and complexity inherent in traditional electronic computing methods [4]. Also, in principle, it would be possible to emulate the functions of the electronic gates in a computational digital circuit with optical logic gates where the optoelectronic counterparts of the FETs (say a light effect transistor (LET) which an M-S-M structure based photodetector that can emulate the characteristics of a FET as will be discussed in detail in Chapter 3) will perform the optically controlled logic switching, and the electrical metal wires can be replaced with optical waveguides [13, 14].

1.2 Objective

Photonic devices can provide advantages in speed and switching energy as compared to electronic counterparts, however, there are three major challenges that photonic devices face when they are directly integrated with electronic devices: size mismatch, energy data rate (EDR), and cascadability [15, 16]. Even though photoconductive devices may potentially offer advantages in switching speed [17] and switching energy [13, 14, 18, 19], it has a major drawback, and hence a photonic device such as the LETs [13, 20], cannot be directly used to drive another LET based circuit since the electrical output of the LET cannot provide the optical input signal that is used drive a similar device. So to simultaneously take advantage of the photonic devices and at the same time avoid the cascading issue in computing applications [20], a hybrid approach has been proposed wherein an integrated circuit only the switching FETs are replaced by LETs. A good example of such a circuit is a 6T static random access memory (SRAM) cell where the access FETs are replaced by LETs, and accordingly the metallic word lines by optical waveguides (OWGs) [14]. Also, this application not only improves the performance of the SRAM but also alleviates

the challenges of size mismatch and EDR (EDR ≤ 10 fJ/bit is desirable for on-chip communication) [15, 16]. This is possible with this approach because it is not required to illuminate each photonic individually, but they can be grouped together and (all access LETs in a row of the 6T array) simultaneously illuminated [14, 20] as in the operation of conventional SRAMs [21].

A novel OWG architecture embedded inside a dielectric layer in the photonic layer with multiple openings into the electronic layer has been designed and simulated using the Synopsys Photonic Design suite, *RSoft* which shows that the proposed OWG system can perform similar functions as the word line of a regular 6T array, by efficiently transmitting optical energy to the LET access devices in the same row. Moreover, the design and implementation of a fully functional hybrid 6T SRAM cell with better noise characteristics compared to the regular 6T cell confirm that the proposed hybrid structure is not only high performing (lesser delay and energy consumption) but also very robust (higher noise stability), which makes the hybrid 6T SRAM a felicitous candidate for cache applications in high performance computing systems.

CHAPTER 2: Optoelectronic Devices

2.1 Overview

Optoelectronics is the combination of optics and electronics which includes the study, design, and manufacture of a hardware device that converts electrical energy into light and vice versa through semiconductors [22]. Optoelectronic devices rely on light-matter interactions and electronic properties of matter to convert light into electrical signals or vice versa. There has always been a drive to improve light-matter interactions in semiconductor materials to make better optoelectronic devices.

In the last decade, one-dimensional or quasi-one-dimensional nanostructures (e.g., nanowires) have been widely researched as potential building blocks for nanoelectronics circuits. Due to their excellent electronic and photonic properties (due to their high surface to volume ratio as a result of a reduction in volume) semiconductor nanostructures (especially nanowires) are being used extensively for photodetectors, optoelectronic switches, optical interconnects, and photovoltaics [23-27]. The optical properties of nanostructures are particularly sensitive to their physical dimensions, and the high surface to volume ratio not only allows for enhanced optical absorption but also enhances carrier confinement which in turn results in a high gain in photodetectors [28, 29]. Due to their excellent electronic and optical properties, and reduced sizes, semiconductor nanowires based electronic-photonic devices are very important building modules for the monolithic integration of nanoelectronic and nanophotonic devices.

Silicon (Si) is the most widely used semiconductor in the IC technology, and silicon nanowires (SiNW) are the most extensively studied for electronic applications. Since Si is the main building block of IC technology, Si-based photodetectors are a lucrative choice for on-chip integration with other electronic devices (for instance FETs), since the whole process flow is

CMOS compatible [23, 24, 30], and the Si photodetectors and other Si-based optical components can be readily fabricated alongside the standard Si FET ICs as shown in Figure 2.1 [30].

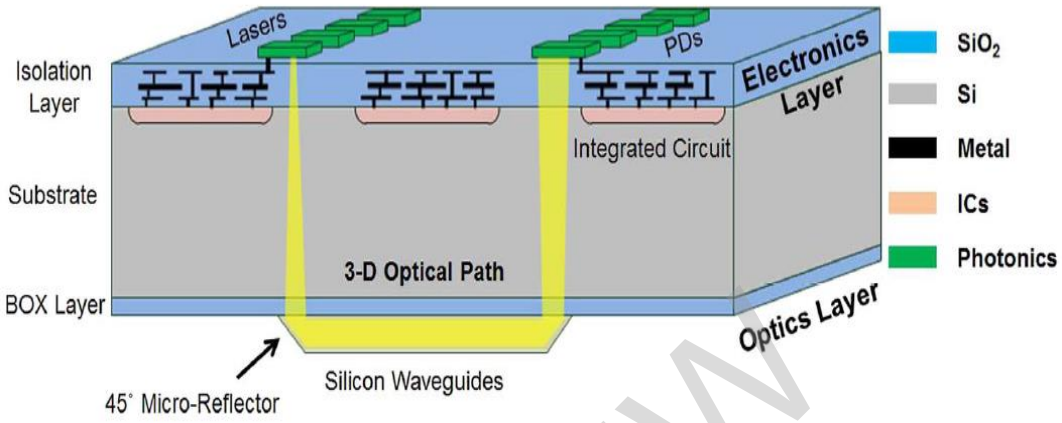

Figure 2.1: SOI-based chip-level optical interconnect module with lasers and photodetectors using 3-D guided-wave path for multi-core processor or memory-to-processor interface [30].

2.2 Nanowire Photodetectors

Photoconductivity is the process of modulation of the electrical conductivity of a device/material due to incident radiation of a suitable wavelength. In the process of photoconductivity, there are several successive or simultaneous mechanisms like the absorption of the incident light depending on the absorptivity of the material, carrier photogeneration, and carrier transport (including carrier trapping, de-trapping, and recombination) through the device to give the photocurrent governed by various physical models [24, 25, 31]. The change in conductivity of a device due to the absorption of radiation of a suitable wavelength mainly depends upon the number of carriers produced per photon absorbed (carrier generation quantum yield), and the mobility of photogenerated carriers (both majority and minority). The duration of the

photoconductive effect leading to the modulation of conductivity depends on the electronic structure of the material (like the presence of traps and defects) which in turn dictates the carrier lifetime of the photogenerated carriers [24]. The high photoresponsivity and gain observed in semiconductor nanowires, and the recent advancement in capturing and understanding the physics behind the photoconduction mechanism in low dimensional systems and materials with a high density of surface states and traps are of huge interest in the potential use of NWs as photo sensing elements in highly integrated optoelectronic devices, optical interconnects, and transceivers. The optical properties of NWs are mainly dependent upon the dielectric functions of bulk materials, with some additional effects like optical birefringence, light scattering, and waveguiding effects (light funneling). However, variations in properties arising from the NW geometry and the low dimensionality leading to carrier confinement also play an important role in the total photoconductivity [24, 31]. The optical birefringence effect mainly depends on the modulation or change of the and also due to the variation of the optical matrix elements due to the quantization of carries and is mainly predominant in very thin NWs with diameter < 10 nm, and due to the confinement of the optical electric field inside the NW's dielectric material. In the case of thin NWs (typically when NW diameter < light wavelength (λ)) the electric field vector's perpendicular component is generally non-dominant while the parallel component dominates, while for thick NWs the electric field distribution inside the NW is non-uniform [24]. Also, enhanced scattering of light happens in NWs when the physical dimension is comparable to or much lesser than the wavelength of incident radiation [24, 31]. It is evident from rigorous numerical calculations that the Silicon NW arrays have a very high absorption of incident light when the wavelength is much greater than that of the fundamental bandgap due to the very high confinement of the electromagnetic energy into the high refractive index of the NW material and its reduced volume,

which is known as light funneling, and thus outperforming their thin film counterparts made from the same material [24, 31].

2.3 Working Mechanism and Carrier Transport

The carrier dynamics and transport phenomena in photodetectors can be described by the combination of Poisson's equation, carrier continuity equations, and the drift diffusion equations as shown below [25, 32, 33]:

$$\nabla^2 \Psi = -\frac{q}{\varepsilon}(p - n + N_D - N_A) \quad (2.1)$$

$$-\frac{1}{q}\nabla . J_n - g + r_n + \frac{\partial n}{\partial t} = 0 \quad (2.2)$$

$$\frac{1}{q}\nabla . J_p - g + r_p + \frac{\partial p}{\partial t} = 0 \quad (2.3)$$

$$J_n = q\mu_n nF + qD_n \nabla \mathrm{n} \quad (2.4)$$

$$J_p = q\mu_p pF - qD_p \nabla \mathrm{p} \quad (2.5)$$

where Ψ is the electrostatic potential; p and n are the total hole and electron concentration after illumination; g is the optical generation rate and $r_{n/p}$ is the electron/hole recombination rate; $\mu_{n/p}$ is the electron/hole mobility; $D_{n/p}$ is the electron/hole diffusion constant, and F is the applied electric field. Under illumination (considering an n-type device), the change in conductivity of the device occurs either due to the change in carrier concertation or change in carrier mobility due to scattering effects is shown [24, 31]:

$$\Delta\sigma = \sigma_{light} - \sigma_{dark} = e(\mu\Delta n + n\Delta\mu) \quad (2.6)$$

Generally, the change in carrier concentration (Δn) due to illumination is much higher than the change in mobility ($\Delta\mu$), and hence neglecting the change in mobility effect, and considering only the recycling gain theory [28], the photocurrent density in an n-type device can be written as:

$$J_{PC} = eF\mu\Delta n \qquad (2.7)$$

The excess carrier depends on the amount of photogenerated carrier which in turn depends on the optical generation rate (number of photo carriers generated per unit volume per unit time due to optical absorption) given by [24, 34]:

$$g = \eta^* \frac{(\frac{P_{opt}}{\hbar\omega})}{volume} \qquad (2.8)$$

where P_{opt} is the absorbed optical power, and it depends on the surface area of the device exposed to illumination and the absorption coefficient of the material, $\hbar\omega$ is the energy of a photon, and η^* is the effective carrier photogeneration quantum efficiency which takes into account the effect of reflection, scattering, and low dimensionality of the NW on optical absorption. Now under steady state and constant illumination, neglecting the effects of excess carrier confinement at the device contacts, and the non-uniform distribution of excess carriers due to the applied electric field [28], the excess carrier concentration may be given as [24, 28]:

$$\Delta n = g\tau \qquad (2.9)$$

where τ is the carrier lifetime and mainly depends on the material properties and the quality of the material used in the device. By combining Equations 2.7 through 2.9, the steady-state photocurrent density for a given wavelength can be written as:

$$J_{PC} = \eta^* \frac{(\frac{P_{opt}}{\hbar\omega})}{volume} eF\mu\tau \qquad (2.10)$$

It is observed from Equation 2.10 that along with other parameters, the photocurrent depends on the quality of the material (τ is generally higher for good quality materials) used in the device. If the effects of both electrons and holes are to be considered, then the total photocurrent density can be written as:

$$J_{PC} = \eta^* \frac{\left(\frac{P_{opt}}{\hbar\omega}\right)}{volume} eF(\mu_n\tau_n + \mu_p\tau_p) \quad (2.11)$$

For a, strictly speaking, MSM photoconductor device, the carrier dynamics under bias are dependent on the potential barrier heights at the two MS contacts, and the voltage drop at the two metal contacts [25, 28, 29]. The asymmetry in the *I–V* curve of these M-S-M structures mainly arises from the difference in potential barrier heights at the two M-S contacts. Under illumination, the increase in current is not only due to the excess carrier concentration (which decreases the series resistance of the NW) but also due to the reduction of the barrier heights at the two M-S contacts [25]. Hence the observation of very high current in single NW-based MSM devices has contribution both from photoconductivity as well as the reduction of the potential barriers at the contacts [25] due to local carrier generation. Also, the recombination at the junctions can be suppressed by the illumination which enhances the photocurrent. It has also been reported that the contribution of contact barrier reduction due to illumination is more pronounced on the photocurrent of the MSM structure than the photoconductive reduction of NW resistance due to the generated excess carriers [25].

Zero bias photo response, similar to that in a solar cell, has been observed in M-S-M structures. The reason may be the formation of a built-in potential barrier at the two contacts due to band bending at the two M-S interfaces which are due to the work functions difference between the metal and the semiconductor contacts [25] at the two ends of the device. In the NW-based M-