INVESTIGATION OF JUNCTION PROPERTIES OF CdS/CdTe SOLAR CELLS AND THEIR CORRELATION TO DEVICE PROPERTIES

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ABSTRACT

Secondary-ion mass spectrometry analysis of the CdS/CdTe interface shows that S diffusion in CdTe increases with substrate temperature and $CdCl_2$ heat treatment. There is also an accumulation of Cl at the interface for $CdCl_2$-treated samples. Modulated photo-reflectance studies shows that devices with $CdCl_2$ heat treatment and open-circuit voltage (V_{oc}) of 835 mV have a distinct high electric-field region in the layer with bandgap of 1.45 eV. Electron-beam induced current measurements reveal a one-sided junction for high V_{oc} devices. The nature of the junction changes with processing. For heterojunction devices, the depletion region includes the highly defective CdS/CdTe interface, which would increase the recombination current and consequently the dark current, leading to lower V_{oc}. In the case of $CdCl_2$-treated cells, the n^+-p junction and its high electric-field results in the junction between structurally compatible CdTe and the Te-rich CdSTe alloy, and thus, in higher V_{oc}.

INTRODUCTION

CdS/CdTe solar cells have been one of the main contenders for thin-film solar cells due to the direct bandgap and ideal bandgap match to the solar spectrum. Major advances in the performance for CdTe cells came in four stages: 1) Introduction of a superstrate structure and the demonstration of devices with reasonable efficiency; 2) Use of a high-temperature close-spaced sublimation (CSS) process and oxygen during growth by the Kodak group to achieve over 10% efficiency [1]; 3) Post-deposition $CdCl_2$ heat treatment for grain growth and type conversion and improved device performance for low-temperature processed films [2]; and 4) The combination of the high-temperature CSS process with $CdCl_2$ heat treatment to achieve 15.8%-efficient devices by the University of South Florida group [3]. The NREL group improved the performance to 16.5% by incorporating a higher-quality transparent conducting oxide (TCO) and buffer layer [4]. Each stage of the performance boost showed a considerable boost in open-circuit voltage (V_{oc}). Presently, the short-circuit current density (J_{sc}) in the devices has been optimized and the loss mechanisms are well identified. On the other hand, V_{oc} of these cells is saturated at 850 mV, which is well below the potential of a 1.5-eV-bandgap semiconductor. Further performance improvement will be possible only by better understanding the factors limiting V_{oc}.

The V_{oc} of the device is influenced to a great extent by the junction properties. The junction region in the superstrate structure used for CdS/CdTe is buried under the CdTe layer and is not easily accessible for measurements. The junction in CdTe/CdS is considered to be a heterojunction between n-type CdS and p-type CdTe. The role of CdS in this device is crucial for achieving the device performance, but is more difficult to understand, given the structural difference and lattice mismatch of over 10%. Interdiffusion between CdS and CdTe has been considered helpful for reducing the effect of the mismatch even though the interface does not exhibit continuous composition grading as a consequence of the miscibility gap in the CdS-CdTe system. Yamamoto et al. [5] have reported on ER studies of CdS/CdTe solar cells. They identified a mixed $Cd_xS_{1-x}Te$ layer and tentatively identified three bandgaps of 1.442, 1.471, and 1.492 eV. Secondary-ion mass spectrometry (SIMS) analysis is heavily influenced by the high surface roughness of their samples, which affects the depth resolution.

We carried out device analysis using modulated photo-reflectance (PR). At NREL, we have developed a polishing technique to prepare samples for SIMS analysis. It helps to minimize the effect of surface roughness and improves the interface resolution. High-resolution electron-beam induced current (EBIC) analysis was carried out on the cross sections of devices to examine the active region of the device. In this paper, we present our preliminary analysis of these results and their correlation to device properties. Detailed results will be presented in a later publication.

EXPERIMENTAL PROCEDURE

CdS/CdTe devices were fabricated in a glass/SnO_2/CdS/CdTe/back-contact structure. CdS films with a nominal thickness of 100 nm were deposited by chemical-bath deposition. CdTe films with a thickness of 8 μm were deposited by CSS at 500°–620°C in He/O_2 ambient. The samples were heat treated with $CdCl_2$ vapor in He/O_2 ambient at 400°C for 5 min. The samples were etched in nitric-phosphoric acid for 30 s prior to application of Cu-doped graphite paste. Contacts were annealed at 270°C for 20 min in He ambient.

SIMS analysis was performed from the CdTe side using a Cameca IMS-3f instrument. The samples were analyzed prior to back-contact application. The samples were polished to reduce root-mean-square (rms) surface roughness from 550 to 5 nm to improve the interface

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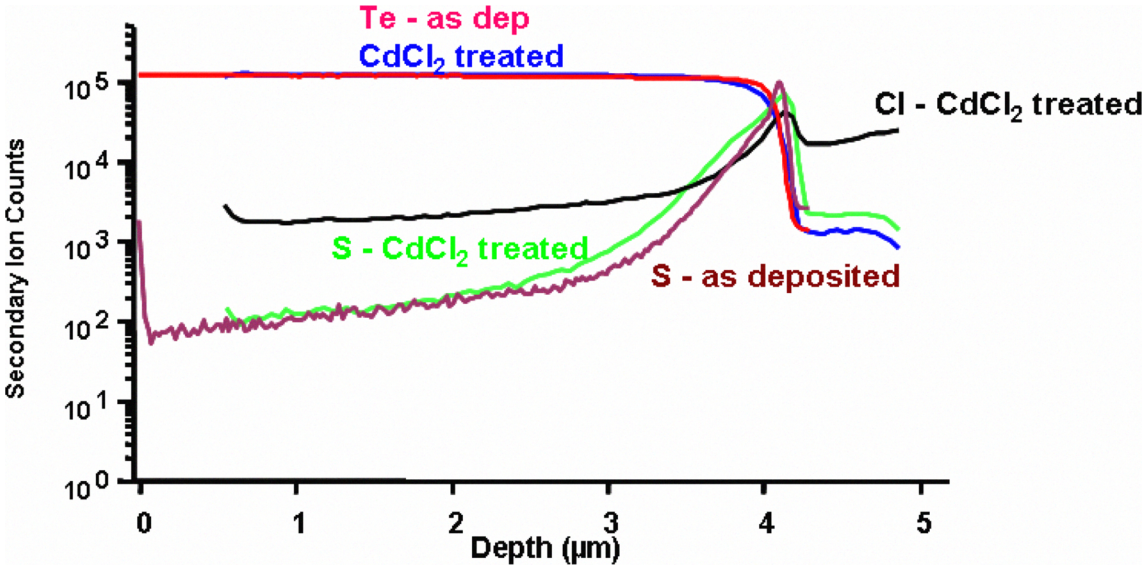

Fig. 1. SIMS profiles for as-deposited and $CdCl_2$-treated samples deposited at 600°C.

resolution, where a 50-nm layer at the interface can be clearly resolved [6].

EBIC measurements were done in a field-emission scanning electron microscope (FESEM JEOL 6320F). Energy transferred from the highly energetic primary electrons (1–40 keV) results in generating a highly localized source of carriers, with a range of penetration R_e. Excess carriers diffuse, and under the field provided by the CdTe/CdS device, those carriers inhibit their recombination and yield a current that is subsequently amplified.

Photo-reflectance is used to probe the electric field at the p-n junction of CdS/CdTe devices. The measurement system consists of a 100-W tungsten lamp, ISA Triax Series 320 spectrometer, Stanford Research Systems SR570 current-preamplifier, and SR30DSP lock-in amplifier. The pump beam is a 532-nm laser, with an attenuated power of ~20 μW, modulated at 400 Hz.

Light and dark current-voltage (I-V) measurements were performed at room temperature using an XT-10 solar simulator adjusted to about an AM 1.5 intensity using a reference CdS/CdTe solar cell.

RESULTS AND DISCUSSION

SIMS

We previously reported on CdS/CdTe structures deposited at 500°–600°C before and after $CdCl_2$ heat treatment [6]. For the untreated samples deposited at 500°C, there is minimal interdiffusion and the interface is nearly abrupt. The interdiffusion increases progressively for the samples deposited at 550° and 600°C. Post - deposition $CdCl_2$ heat treatment increases the interdiffusion, particularly for samples deposited at lower temperature. For $CdCl_2$-treated samples, we have seen accumulation of Cl at the CdS/CdTe interface. Figure 1 shows the SIMS profile for a sample deposited at 600°C before and after $CdCl_2$ heat treatment. This sample shows considerable S diffusion in the CdTe layer for the as-deposited case, and the S profile does not change greatly after $CdCl_2$ heat treatment. There is Cl accumulation at the interface for the $CdCl_2$-treated sample. We also observe predominant diffusion of CdS in CdTe. One-sided diffusion is deduced from both SIMS and quantum efficiency (QE) results. SIMS analysis shows the presence of a distinct CdS layer at the interface. QE analysis of the devices shows a quantum loss corresponding to CdS bandgap, and the magnitude of this loss corresponds to the thickness of the remaining CdS layer.

SIMS analysis results are summarized as follows:

1) Diffusion of CdS into CdTe is a function of both substrate temperature and post-deposition $CdCl_2$ heat treatment.

2) Sulfur diffusion increases with substrate temperature for as-deposited samples. For as-deposited samples deposited at 500°C, there is negligible diffusion and the metallurgical interface is almost abrupt.

3) Post-deposition $CdCl_2$ heat treatment enhances the interdiffusion at the interface. The effect of the heat treatments is maximized for smaller-grain samples deposited at lower substrate temperature. On the other

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hand, for samples deposited at 600°C, most of the diffusion takes place during deposition.

4) There is accumulation of Cl at the CdS/CdTe interface for $CdCl_2$-treated samples. The level of Cl in the bulk of CdTe is lower in samples deposited at lower temperatures. This is most likely due to the grain-size effects, because the grain size for samples deposited at lower temperatures is smaller.

5) Sulfur preferentially diffuses in CdTe as compared to tellurium in CdS. For example, sulfur diffuses 300–500 nm in CdTe, and a CdS layer of 50 nm remains in $CdCl_2$-treated samples out of the initial 100-nm CdS layer.

Modulated Reflectance

We have used modulated reflectance analysis to determine the location and magnitude of the electric field in the device. We measured different samples with and without a CdS layer. Figure 2 shows the photo-reflectance spectrum of a CdTe thin-film solar cell, measured at room temperature. This sample was deposited at a substrate temperature of 620°C and treated in $CdCl_2$ vapor at 400°C for 5 min. The cell had an efficiency of 13.5% with a V_{oc} of 835 mV. Broadened Franz-Keldysh oscillations (FKOs) are clearly observed in the spectrum. The data were fitted to a generalized FKO lineshape function with a broadening parameter [7], which yields a bandgap of 1.448 eV and an electric field of 31.9 kV/cm. This is the first measurement of the junction field in CdS/CdTe solar cells. For a device without CdS layer, the reflectance spectrum indicates a bandgap of 1.5 eV. Therefore, the bandgap of 1.448 eV observed for the CdS/CdTe solar cell corresponds to the intermixed CdSTe alloy on the Te-rich side [8]. A similar modulation spectrum of electroreflectance was reported previously [4], but the data were fitted with a multiple-bandgap model and a low-field lineshape function. We believe that the strong-field lineshape is more appropriate for the spectrum.

EBIC

EBIC observations performed at extremely low e-beam excitation power (E_b = 1 keV, I_b = 100 pA) provide a highly localized source of electron-hole pairs (about 20 nm), resolving the features at the CdTe/CdS interface. The SEM micrograph in Fig. 3a shows in detail the SnO_2/CdS/CdTe structure. The measured induced current shown in Fig. 3b is for the high-efficiency, thin-film CdTe solar cell used for the analysis in Fig. 2. EBIC imaging at such high resolution confirms that the CdS layer does not show any EBIC activity. The maximum induced current is well defined close to the metallurgical interface in the intermixed layer at the interface. We expect the EBIC maximum to be at the point of maximum electric field. If we assume that the current collection is primarily field-assisted collection, then we can estimate the depletion width at the junction from the EBIC spectrum. Estimates of the recombination velocity at the CdTe/CdS interface (S/D) are between 10 and 10^3 cm^{-1} for higher-efficiency cells. However, depending on the extent of the CdTe/CdS

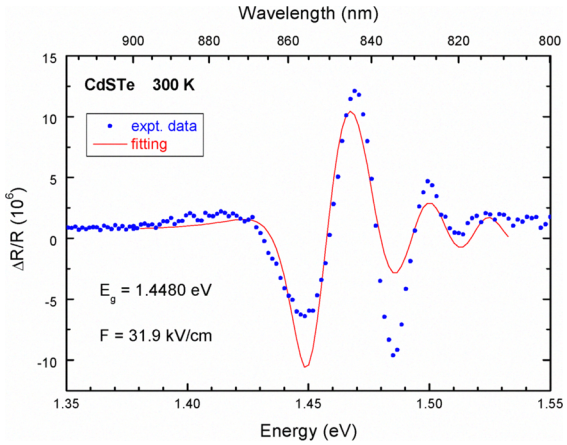

Fig. 2. Photo-reflectance spectrum of a CdTe thin-film solar cell, showing multiple Franz-Keldysh oscillations due to the existence of a strong electric field in a p-n junction.

interdiffusion or the chemistry of the CdS film, we have estimated increases in S/D of up to 10^6 cm^{-1}, although the CdTe/CdS interface can still be modeled as an ideal heterojunction. The increase in S/D should result in a poor quantum efficiency at short wavelengths.

An extreme degradation in photoconversion efficiency is accompanied by the degradation of the resolution of the induced current at the CdTe/CdS interface. A low-temperature sample deposited at 475ºC after a high-temperature (450ºC) $CdCl_2$ vapor treatment consumes almost all of the CdS layer with the consequent S outdiffusion into the CdTe film. The main contribution to the EBIC is from the CdTe/CdS interface of the remaining CdS.

The EBIC signal in the Fig. 3b mainly extends in the CdTe layer for about 3 μm. Capacitance-voltage (C-V) measurements on this device predict a depletion width of about 3 μm, which supports our assumption that the current collection in these cells is primarily field assisted. Assuming the depletion width on the p-side is 3 μm and using a maximum field of 31.9 kV/cm (determined from modulated reflectance studies), we estimate a hole carrier concentration on the p-side to be $5.5x10^{14}$ cm^{-3}. We carried out EBIC analysis on several samples and found a similar pattern for high-efficiency CdTe devices prepared by different techniques. Considering that the maximum of the electric field in the depletion region is at the p-n junction and assuming that the maximum of the EBIC signal occurs at the maximum field point, we estimate the depletion width on the side to be on the order of 100 nm based on the extent of the EBIC signal toward the metallurgical junction. This gives an electron carrier density on the order of $1.65x10^{16}$ cm^{-3}. Thus, we have essentially one side junction, with the electrical junction at an intermixed alloy with a bandgap of 1.448 eV. Based on the data of Ohata et al. [8], this corresponds to an alloy

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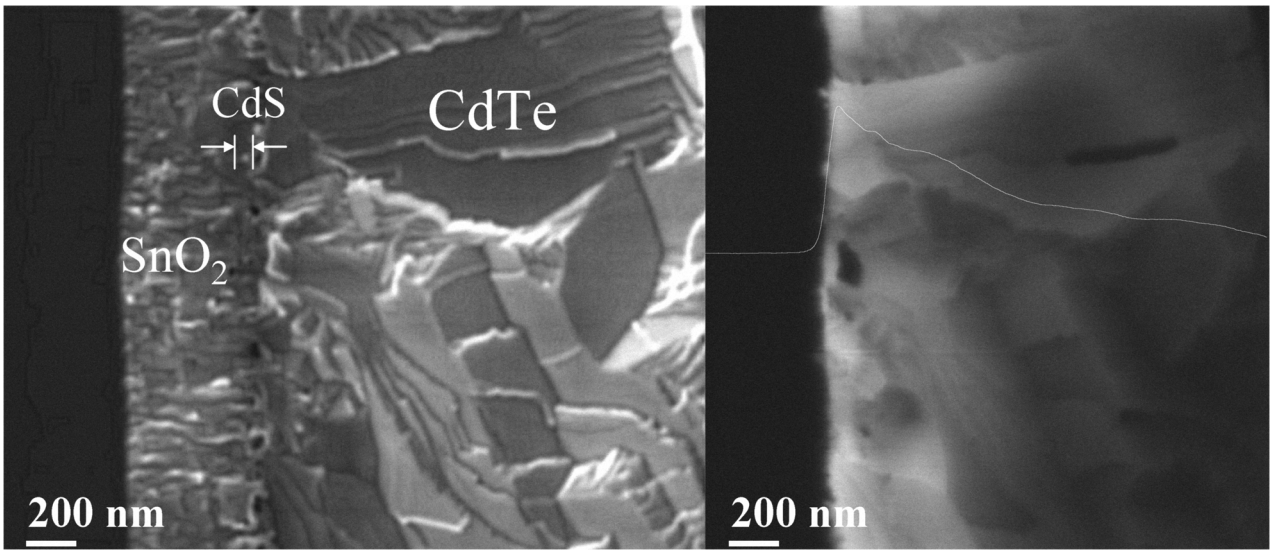

Fig. 3. SEM micrograph (left) and high-resolution EBIC image (right) of CdS/CdTe junction for a high-efficiency device.

composition of approximately $CdS_{0.1}Te_{0.9}$. Although there is a second possible alloy composition with higher S content, its presence is unlikely due to the miscibility gap in the CdS-CdTe alloy system.

The hole carrier concentration of $5.5x10^{14}$ cm^{-3} estimated here agrees with the values reported in the literature. Electron density on the order of 10^{16} cm^{-3} can be explained physically based on the following observations.

Intermixing of CdS and CdTe layers at the interface mainly occurs during deposition at high temperatures because the SIMS profile does not change significantly for the $CdCl_2$-treated sample. The formation of vacancies at S or Te sites could form during intermixing, leading to n-type doping. For $CdCl_2$-treated samples, SIMS analysis shows an accumulation of Cl at the metallurgical interface, where the intermixed alloy is located. Because Cl is an n-type dopant in II-VI compounds, it could dope the alloy layer. We will pursue further compositional analysis to get a quantitative estimate of the level of Cl.

Device Model

Based on the results presented here, we propose the following model for high-efficiency solar cells with V_{oc} beyond 800 mV. The p-n junction is between the Te-rich CdSTe layer and CdTe layer. The depletion width extends mainly on the CdTe side, where the doping level is considerably lower. Assuming field-assisted carrier collection, we do not expect collection from the CdS layer. The junction occurs between the structurally compatible CdTe and $CdS_{0.1}Te_{0.9}$ alloy layer and can be considered a quasi-homojunction. Reducing the structural defect density could lead to a reduction of charged defect density, thus reducing the recombination current in the depletion region and dark current in the device. The CdTe device with highest reported V_{oc} of 890 MV is predicted to be a buried homojunction [9]. For CdS/CdTe devices deposited without $CdCl_2$ heat treatment, the best V_{oc} achievable is 750 mV. In this device, the depletion layer extends to the CdS interface, which has a higher defect density due to incompatible structures and large lattice mismatch. In the future, we will publish a more detailed analysis of devices prepared under different conditions and their device properties based on the device model presented here.

CONCLUSIONS

Modulated reflectance analysis of high-efficiency CdS/CdTe devices shows the presence of a high field region of 32 kV/cm in the $CdS_{0.1}Te_{0.9}$ alloy layer. Cross-sectional EBIC measurements on these devices predict a one-sided junction between a structurally compatible CdTe and $CdS_{0.1}Te_{0.9}$ alloy layer. SIMS data on the $CdCl_2$-treated CdS/CdTe structure show the accumulation of Cl at the interface, which could dope the alloy layer n-type to produce a one-sided quasi-homojunction. Reduced charge density in the depletion region could be responsible for the higher V_{oc} observed in these devices.

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