Comparison of CMOS Current Conveyor Circuits for Non-Foster Applications

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***Abstract*— Current conveyors are an important component for implementing non-Foster circuits such as negative capacitors and negative resistors. However, different topologies exist for implementing negative capacitance using a current conveyor, and the performance of such topologies can vary greatly. Therefore, this paper considers two competing realizations of negative capacitance using a current conveyor, where both circuits are designed for -5 pF in a 0.5 micron CMOS process. Simulation results are presented that show significant bandwidth differences for the two -5 pF designs, where one approach has more than twice the bandwidth of the second approach.**

Keywords—negative capacitance; negative impedance converter; CMOS; bandwidth; second generation current conveyor (CCII+).

I. INTRODUCTION

A current conveyor is a basic building block that has found wide application since its introduction in 1968 by Smith and Sedra [1] and the reformulation in 1970 by Sedra and Smith [2]. Current conveyors have found use in current-mode and mixed-mode filter design, instrumentation and wideband amplifiers, and non-Foster circuits [3]-[5], [7]-[8]. Although current conveyors have been used for more than four decades, there is renewed interest in their use in a variety of analog signal processing tasks such as oscillators, controlled sources, impedance convertors, impedance inverters, gyrators, and various analog computation elements. The present paper compares two topologies of current conveyors for relative bandwidth performance in a 0.5 micron CMOS process for non-Foster applications. In this, simulation results show marked differences in bandwidth as noted for other processes [6].

There are several generations of current conveyors with different sets of equations describing current and voltage relationships at the terminals of the devices. In this paper, second-generation current conveyors (CCII) are considered for the realization of negative capacitance using two different circuit topologies. Although the same current conveyor is used in both topologies, simulation results are given that show one approach has twice the bandwidth of the other.

In the following section, the second-generation CMOS current conveyor is described, and the two competing circuit topologies for negative capacitance are described. The subsequent section describes the detailed design, layout, and simulation results for the proposed circuits. The simulation results demonstrate significant performance differences between the two competing topologies when compared for a nominal design goal of -5 pF.

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II. CIRCUIT ANALYSIS

The CCII current conveyor to be investigated is based on a Sedra and Smith second-generation current conveyor [2], and is shown in Fig. 1. It is a three-port device with the following set of equations:

$$v_x = v_y \,, \tag{1}$$

$$i_y = 0 \,, \tag{2}$$

$$i_z = i_x \,, \tag{3}$$

where v_x and i_x are the input voltage and current to the X terminal, v_y and i_y are the input voltage and current to the Y terminal, and v_z and i_z are the input voltage and current to the Z terminal of Fig. 1. The sign of the current i_z in (3) determines the positive or negative type of second-generation current conveyor (CCII). As given in (3) above, and in the following discussion, a positive CCII device (CCII+) is used.

The first negative capacitance circuit topology under consideration is shown in Fig. 2, where the Z terminal is connected to the Y terminal. The same point also serves as the input of the overall circuit, having input impedance Z_{in} with respect to ground. A load impedance Z_L is connected from terminal X to ground, and serves as the reference impedance that is to be inverted.

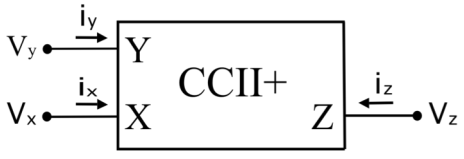

Fig. 1. Basic CCII+ current conveyor voltages and currents.

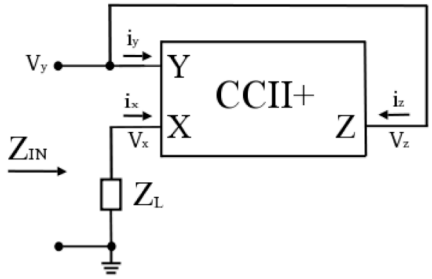

Fig. 2. First negative capacitance circuit topology using a CCII+ current conveyor. Input impedance Z_{in} is between terminal Y and ground, and load impedance Z_L is between terminal X and ground, where $Z_{in} = -Z_L$.

From the node at terminal X in Fig. 2,

$$i_x = -\frac{v_x}{Z_L} \ , \tag{4}$$

and since $i_z = i_x$ from (3), and since $v_x = v_y$. from (1), then

$$i_z = -\frac{v_y}{Z_L} \ . \tag{5}$$

At the input terminal, Y, the input voltage $v_{in} = v_y$, and since $i_y = 0$ from (2), summing currents at terminal Y yields $i_{in} = i_z$, and so (5) becomes

$$i_{in} = -\frac{v_{in}}{Z_L} \ , \tag{6}$$

and the input impedance Z_{in} is

$$Z_{in} = \frac{V_{in}}{i_{in}} = -Z_L \ . \tag{7}$$

The second negative capacitance circuit topology under consideration is shown in Fig. 3, where the Z terminal of the CCII+ is connected to the Y terminal, and now the X terminal serves as the input terminal of the circuit having input impedance Z_{in} with respect to ground. A load impedance Z_L is

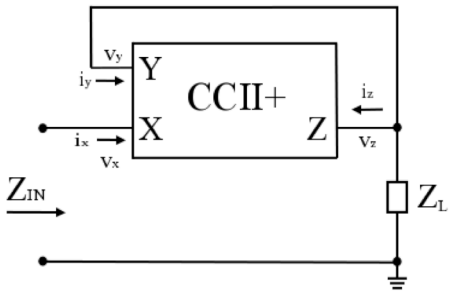

Fig. 3. Second negative capacitance circuit topology using a CCII+ current conveyor. Input impedance Z_{in} is between terminal X and ground, and load impedance Z_L is between terminal Z and ground, where $Z_{in} = -Z_L$.

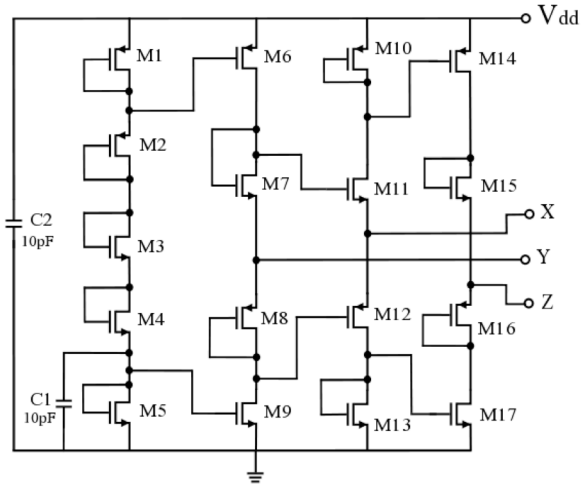

Fig. 4. Detailed schematic of current conveyor circuit (CCII+).

also connected from the Z terminal to ground, where Z_L serves as the reference impedance to be inverted.

For the circuit of Fig. 3, since $i_y = 0$ from (2), then

$$i_z = -\frac{v_z}{Z_L} \ . \tag{8}$$

From (1) the input voltage $v_{in} = v_x = v_y = v_z$, and $i_z = i_y$ from (3), so rearranging, (8) becomes

$$Z_{in} = \frac{V_x}{i_x} = \frac{V_{in}}{i_{in}} = -Z_L \ . \tag{9}$$

III. Results

The detailed schematic of the CMOS implementation of the CCII+ current conveyor is shown in Fig. 3, where all pMOS are 100×0.5 microns and all nMOS are 50×0.5 microns. The layout of the CCII+ of Fig. 4 in 0.5 micron CMOS is shown in Fig. 5, and the design is currently out for fabrication.

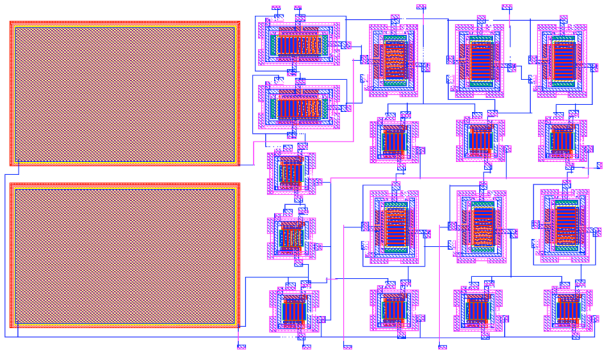

Fig. 5. Layout of current conveyor (CCII+) circuit in 0.5 micron CMOS.

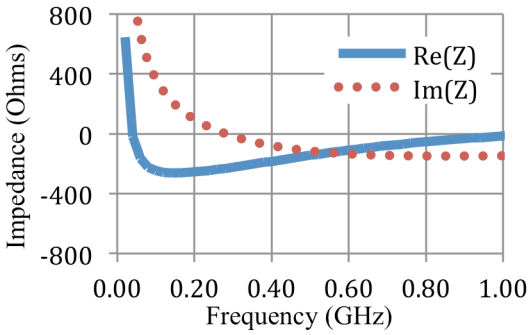

Fig. 6. Simulation results showing real part of Z_{in} (solid blue) and imaginary part of Z_{in} (dotted red) for a 5 pF capacitive load Z_L for the circuit of Fig. 2.

To compare the performance of the two topologies of Fig. 2 and Fig. 3, the two designs were simuluated with a 5 pF load for Z_L. In this case, both circuits then have an expected input impedance Z_{in} corresponding to a -5 pF negative capacitance.

The simulation results for Z_{in} of the circuit in Fig. 2 are shown in Fig. 6, with the real part of Z_{in} shown in solid blue and the imaginary part of Z_{in} shown in dotted red. As is evident in Fig. 6, the imaginary part of the impedance follows the expected profile of a negative capacitance, where the sign of the reactance is inverted from that a of a positve capacitance. The simulation results for Z_{in} of the circuit in Fig. 3 are shown in Fig. 7.

The resulting capacitances at the inputs of the circuits of Fig. 2 and Fig. 3 are shown in Fig. 8 and Fig. 9, respectively. As seen in the simulation results of Fig. 8 and Fig. 9, the capacitance values are near their expected values of -5 pF at low frequency, with corresponding low-frequency capacitances of -4.1 pF and -5.7 pF respectively. However, comparing the results of Fig. 8 and Fig. 9, the circuit of Fig. 3 has substantially larger bandwidth than the circuit of Fig. 2.

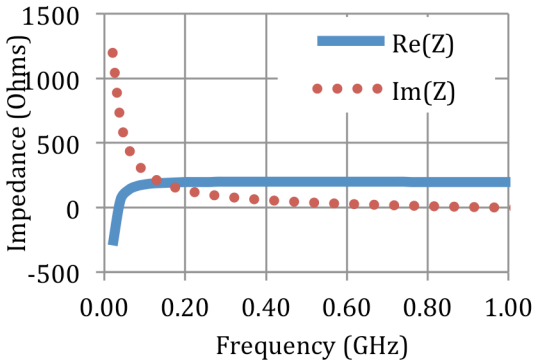

Fig. 7. Simulation results showing real part of Z_{in} (solid blue) and imaginary part of Z_{in} (dotted red) for a 5 pF capacitive load Z_L for the circuit of Fig. 3.

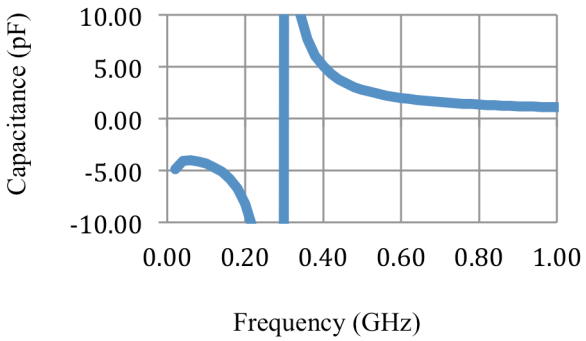

Fig. 8. Simulation results showing input capacitance observed at Z_{in} for a load capacitance Z_L of 5 pF for the topology of Fig. 2 (computed capacitance values above the resonance near 300 MHz are anomalous due to zero crossing of Im(Z)).

Finally, as is typical with many non-Foster circuits, the two circuits were observed to be sensitive to the impedances of the signal sources used in the simulation. Although not evident in the results of Fig. 8 and Fig. 9, the circuit of Fig. 2 used a source impedance of 50 ohms and the circuit of Fig. 3 was tested with a 2500 ohm source impedance. To illustrate this, the circuit of Fig. 10 is a representative model of the input impedance of the circuit of Fig. 3 with impedance of Fig. 7. In Fig. 10, R_p = -2500 Ω, R_s = 180 Ω, and C = -6 pF. The circuit of Fig. 10 approaches an impedance of Z_{in} = 180 Ω, at high frequency, just as the simulation of Fig. 7. At dc, the circuit of Fig. 10 approaches an impedance of Z_{in} = -2320 Ω, corresponding to the downward trajectory of Re(Z) seen at the lowest frequency of Fig. 7. Thus, a source impedance greater than 2320 ohms was used for the circuit of Fig. 3 to ensure stable simulations at low frequency [9].

IV. Conclusion

Two different circuit topologies for negative capacitance were simulated using second-generation CMOS current conveyors

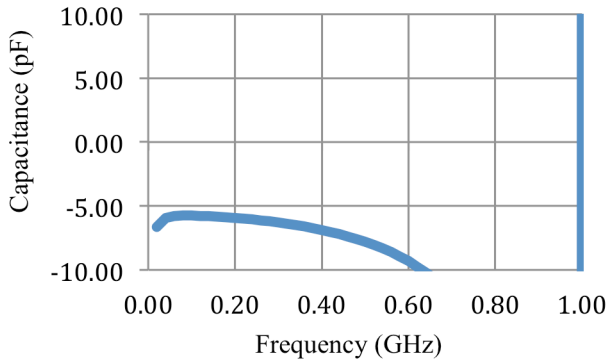

Fig. 9. Simulation results showing input capacitance observed at Z_{in} for a load capacitance Z_L of 5 pF for the topology of Fig. 3 (computed capacitance values above the resonance near 1000 MHz are anomalous).

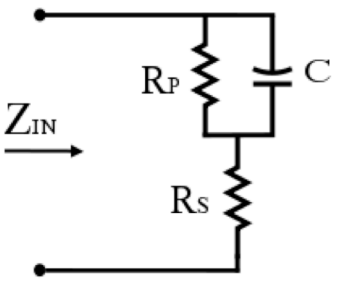

Fig. 10. Circuit model for input impedance Z_{in} of the topology of Fig. 3 with impedance of Fig. 7.

(CCII+). The analysis of the circuits, under simplifying assumptions, shows that the expected observed negative capacitances should approximately equal the negative of the load capacitances. The simulation results are in good agreement for the 5 pF external load, with observed negative capacitances of -4.1 pF and -5.7 pF at low frequency. However, one topology is observed to have more than twice the bandwidth of the other, even though the same CMOS CCII+ is used in both cases. The only difference between the two cases is the configuration of the circuitry external to the CCII+.

ACKNOWLEDGMENT

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REFERENCES

[1]. K. C. Smith and A. Sedra, “The current conveyor - A new circuit building block,” Proceedings of the IEEE, vol. 56, no.8, pp. 1368-1369, Aug. 1968.

[2]. A. Sedra and K. C. Smith, “A second generation current conveyor and its applications,” IEEE Trans. on Circuit Theory, vol.17, no.1, pp. 132-134, Feb. 1970.

[3]. M. T. Abuelma’atti and A. Bentrcia, “A novel mixed-mode CCII-based filter,” Active and Passive Electronic Components, vol. 27, pp. 197-205, Dec. 2004.

[4]. C. Galanis and I. Haritantis, “An improved current mode instrumentation amplifier,” Proceedings of the third IEEE international conference on Electronics, Circuits and System, vol. 1, pp. 65-68, Oct. 1996.

[5]. T. P. Weldon, K. Miehle, R. S. Adams and K. Daneshvar, "A wideband microwave double-negative metamaterial with non-Foster loading," 2012 Proceedings of IEEE SoutheastCon, pp. 1-5, 15-18, Mar. 2012.

[6]. J. Popovic, A. Pavasovic, and D. Vasiljevic, “Low-power High Bandwidth CMOS Current Conveyor,” PROC 21st International Conference on Microelectronics (MIEL’97), vol. 2, Yugoslavia, Sep. 1997.

[7]. W. Surakampontorn, V. Riewruja, K. Kumwachara and K. Dejhan, “Accurate CMOS-based current conveyors,” IEEE Trans. Instvum. Meas., vol. 40, no. 4, pp. 699-702, Aug. 1991.

[8]. A. S. Sedra, G.W. Roberts and F. Gohh, “The current conveyor: history, progress and new results,” IEE Proc. of ISCAS 1990, Vol. 137, pp 78-87

[9]. S. D. Stearns, “Non-Foster circuits and stability theory,” 2011 IEEE International Symposium Antenas and Propagation (APSURSI), pp. 1942-1945, Jul. 2011.