An Ultralow-Power Low-Noise CMOS Biopotential Amplifier for Neural Recording

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***Abstract*—This brief presents a design strategy for a neural recording amplifier array with ultralow-power low-noise operation that is suitable for large-scale integration. The topology combines a highly efficient but supply-sensitive single-ended first stage with a shared reference channel and a differential second stage to effect feedforward supply noise cancellation, combining the low power of single-ended amplifiers with improved supply rejection. For a two-channel amplifier, the measurements show a midband gain of 58.7 dB and a passband from 490 mHz to 10.5 kHz. The amplifier consumes 2.85 μA per channel from a 1-V supply and exhibits an input-referred noise of 3.04 $\mu\mathrm{V_{rms}}$ from 0.1 Hz to 100 kHz, corresponding to a noise efficiency factor of 1.93. The power supply rejection ratio is better than 50 dB in the passband. The amplifier is fabricated in a 90-nm CMOS process and occupies 0.137 mm^2 of chip area.**

***Index Terms*—Current-reuse complimentary-input (CRCI) amplifier, low noise, neural amplifier, noise efficiency factor (NEF), power supply rejection ratio (PSRR), ultralow power.**

I. Introduction

RAPID advances in implantable integrated neural recording systems have allowed neuroscientists and clinicians to treat neurological disorders, such as epilepsy, Parkinson's disease, and spinal cord injuries. Large multichannel recording systems (e.g., [1]) are capable of observing many neurons simultaneously. However, because thermal dissipation and wireless power delivery limitations constrain the total allowable power dissipation, large arrays must limit the power consumption of each channel. The small amplitude of extracellular action potentials requires input-referred amplifier noise of no more than 5–10 $\mu\mathrm{V_{rms}}$ to avoid degraded signal quality [2]. Because amplifier power is inversely related to the squared input-referred noise voltage $v^2{}_{\mathrm{ni}}$, the simultaneous constraints on noise and power impose a challenging design tradeoff.

Recent advances in low-power low-noise CMOS biopotential amplifiers have been reported in [3]–[10]. The capacitive feedback approach proposed in [3] that uses capacitors to set the gain and to achieve dc offset rejection has become the most popular topology in building biopotential amplifiers. Noise-power efficiency has been further improved by employing current scaling [4] and current splitting [5] techniques in folded-cascode operational transconductance amplifiers (OTAs). However, the severe current scaling scheme between the input differential pairs and the folded branches requires that current errors caused by mirroring be well controlled. Additionally, the voltage headroom required by the large source degeneration increases the minimum supply voltage.

An open-loop single-ended current-reuse complimentary-input (CRCI) amplifier [6] demonstrated very high power efficiency but suffered from poor linearity and supply rejection. Because of the poor power supply rejection ratio (PSRR), low-noise voltage regulation circuitry may be required, which consumes additional power and potentially increases the design complexity. Recently, a closed-loop fully differential CRCI amplifier has been presented in [7], in which the PSRR was greatly improved. However, at a given power budget, the input-referred thermal noise power was twice that of the single-ended amplifier [6] because the output noise was doubled by the differential branches, which significantly degraded the noise-power efficiency.

This brief presents a two-stage amplifier configuration combined with CRCI technique and sharing architecture, which achieves a very good power-noise tradeoff and adequate PSRR. The ac-coupled input rejects large dc offsets generated at the electrode–tissue interface. This brief is organized as follows. Section II describes the proposed architecture and the design considerations, including the analysis of PSRR, noise optimization, and noise efficiency factor (NEF) calculation. Section III presents the experimental results and biological recordings. Finally, Section IV concludes this brief.

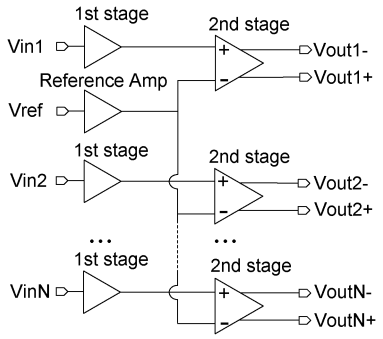

Fig. 1. Configuration of the proposed biopotential amplifier.

II. Neural Amplifier Design

A. Overall System Design

Fig. 1 shows the configuration of our proposed biopotential amplifier. The first-stage amplifier is a single-ended CRCI

Manuscript received October 30, 2014; revised February 6, 2015; accepted June 12, 2015. Date of publication July 17, 2015; date of current version September 25, 2015. This work was supported in part by the National Science Foundation under Grant DBI-1152361. This brief was recommended by Associate Editor B. Choubey.

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Digital Object Identifier 10.1109/TCSII.2015.2457811

amplifier [6] with capacitive feedback, which achieves very high power-noise efficiency but poor PSRR. In order to improve the PSRR, we employ a reference amplifier (shared by N channels) which is identical to the first stage. The second stage is a fully differential OTA with capacitive feedback. The supply noise, which is equally coupled to the outputs of the first stage and the reference, is suppressed as a common-mode signal by the second stage. The sharing architecture of the reference amplifier results in a significant reduction of power dissipation. By using this approach, the amplifier achieves good PSRR while keeping superior noise-power efficiency.

Assuming that the first stage and the reference amplifier are perfectly matched, the ideal PSRR of the whole amplifier can be expressed as

$$\text{PSRR}_{\text{ideal}} = \frac{A_{v1} \cdot A_{v2}}{A_{s1} \cdot A_{\text{cm2}}} = \text{PSRR}_1 \cdot \text{CMRR}_2 \tag{1}$$

where A_{v1} is the signal gain of the first stage, A_{s1} is the supply noise gain of the first stage, A_{v2} and A_{cm2} are the differential-mode gain and common-mode gain of the second stage, respectively, PSRR_1 is the PSRR of the first stage, and CMRR_2 is the common-mode rejection ratio of the second stage.

Taking the mismatch between the first stage and the reference amplifier in to consideration, (1) can be modified as

$$\text{PSRR} = \frac{A_{v1} \cdot A_{v2}}{\Delta A_{s1} \cdot A_{v2} + A_{s1} \cdot A_{\text{cm2}}} \tag{2}$$

where ΔA_s represents the supply noise gain mismatch between the first stage and the reference. If the supply noise gain mismatch (ΔA_s) is sufficiently small, (2) can be reduced to (1).

Using a similar approach, the CMRR of the whole amplifier can be expressed as

$$\text{CMRR} = \frac{A_{v1} \cdot A_{v2}}{\Delta A_{v1} \cdot A_{v2} + A_{v1} \cdot A_{\text{cm2}}} \tag{3}$$

where ΔA_{v1} represents the signal gain mismatch between the first stage and the reference.

Assuming that the first stage and the reference amplifier are identical $(I_1 = I_{\text{REF}})$, the total current consumption per channel can be expressed as

$$I_{\text{tot}} = I_1 + \frac{I_{\text{REF}}}{N} + I_2 = \frac{N+1}{N} I_1 + I_2 \tag{4}$$

where I_1, I_{REF}, and I_2 represent the current consumption of the first stage, the reference amplifier, and the second stage, respectively, while N is the number of channels.

Considering that the first stage and the reference amplifier are identical $({v^2}_{\text{ni1}} = {v^2}_{\text{niREF}})$ and the gain of the first stage A_{v1} is set to be sufficiently large, the input-referred noise power of each amplifier can be calculated as

$$v_{\text{ni}}^2 = v_{\text{ni1}}^2 + v_{\text{niREF}}^2 + \frac{v_{\text{ni2}}^2}{A_{v1}^2} \approx 2v_{\text{ni1}}^2 \tag{5}$$

where ${v^2}_{\text{ni1}}$, ${v^2}_{\text{niREF}}$, and ${v^2}_{\text{ni2}}$ represent the input-referred noise powers of the first stage, the reference amplifier, and the second stage, respectively, while A_{v1} is the gain of the first stage.

Typical extracellular action potentials have frequency content ranging from 100 Hz to 7 kHz [9]. In order to accurately capture spiking activity, this amplifier was designed to have bandwidth extending up to 10 kHz.

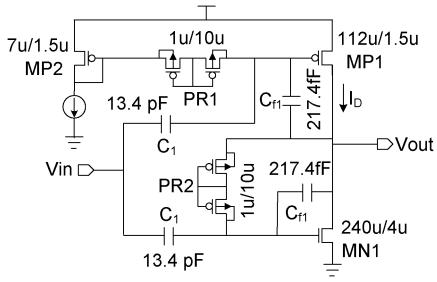

Fig. 2. Schematic of the first-stage amplifier.

B. First-Stage Design

The schematic of the first-stage amplifier is shown in Fig. 2. In order to reject the large dc offsets generated at the electrode–tissue interface, MOS-bipolar pseudoresistors [3] with high resistances and on-chip capacitors are employed. The incremental resistance of the pseudoresistors is extremely high $(> 100\ \text{G}\Omega)$ [3] when the voltage across it is small $(|\Delta V| < 0.2\ \text{V})$. The open-loop single-ended CRCI amplifier [6] can give superior noise performance for a given power budget at the expense of reduced linearity and imprecise gain control. According to (2) and (3), the gain mismatch between the first stage and the reference amplifier should be minimized to achieve good PSRR and CMRR. To improve gain accuracy and linearity, capacitive feedback [3] is used in the first stage and reference amplifier. The midband gain A_{v1} of the first-stage amplifier is set by C_1/C_{f1}. In order to achieve sufficient matching for the required PSRR and CMRR, the capacitors (C_1 and C_{f1}) are large and carefully laid out, occupying 45% of the chip area in this design.

By driving the gates of both PMOS and NMOS input transistors, the CRCI technique reuses the current and doubles the effective transconductance, significantly reducing the input-referred noise. Additionally, transistors $MN1$ and $MP1$ are sized large enough to reduce the flicker noise to an acceptable level. The aspect ratios of $MN1$ and $MP1$ are chosen for weak inversion operation in order to maximize g_m/I_D. Finally, the RC network formed by the pseudoresistor and the ac-coupling capacitor at the gate of $MP1$ presents a low-pass characteristic to filter out most of the noise from the current reference $MP2$ and the pseudoresistor PR1.

Assuming that thermal noise contribution is dominant and according to the design guidelines presented in [11], analysis of this circuit reveals that the input-referred noise power of the first-stage amplifier can be expressed as

$$\begin{aligned}\frac{{v^2}_{\text{ni1}}}{\Delta f} = &\left(\frac{C_1 + C_{\text{f1}}}{C_1}\right)^2 \cdot \left[\frac{2kT}{\kappa(g_{mn1} + g_{mp1})}\right] \\ &+ \left(\frac{C_{\text{f1}}}{C_1}\right)^2 \cdot \frac{4kTR_{\text{PR}}}{\left(1 + sC_{\text{f1}}R_{\text{PR}} - \frac{sC_1R_{\text{PR}}}{g_{mn1}(r_{on1} \| r_{op1})}\right)^2} \\ &+ \left(\frac{C_1 + C_{\text{f1}}}{C_1}\right)^2 \cdot \left(\frac{g_{mp1}}{g_{mp1} + g_{mn1}}\right)^2 \\ &\cdot \left(\frac{1}{1 + sC_1R_{\text{PR}}}\right)^2 \cdot \left(4kTR_{\text{PR}} + \frac{2kT}{\kappa g_{mp2}}\right)\end{aligned} \tag{6}$$

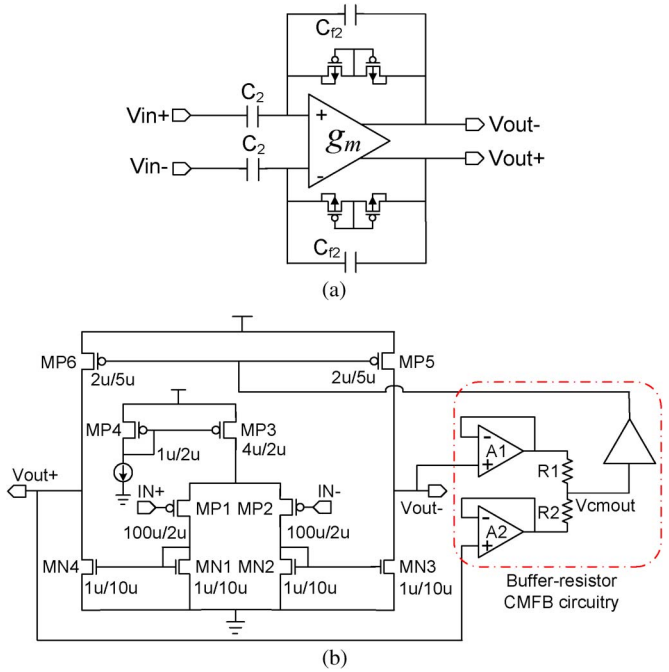

Fig. 3. (a) Schematic of the second-stage amplifier. (b) Schematic of the OTA.

where $g_{mn1}, g_{mp1,2}$ are the transconductances of the transistors $MN1$, $MP1$, and $MP2$, respectively, r_{on1} and r_{op1} are the output resistances of the transistors $MN1$ and $MP1$, respectively, $R_{\rm PR}$ represents the equivalent resistance of the pseudoresistors, and κ is the reciprocal of the subthreshold slope factor n_p. The last two items in (6) represent the noise contributions from the pseudoresistors and the current reference $MP2$, which are filtered by the pseudoresistor and feedback capacitor. In order to minimize the noise contributions from the pseudoresistors and the current reference $MP2$, long-channel ($L = 10\ \mu$m) pseudoresistors are used to increase their equivalent resistance. Assuming that $g_{mn1} = g_{mp1} = g_m$ and the noise contributions from the pseudoresistors and the current reference $MP2$ is negligible, (6) then reduces to

$$\frac{v_{\rm ni1}^2}{\Delta f} \approx \left(\frac{C_1 + C_{\rm f1}}{C_1}\right)^2 \cdot \left(\frac{kT}{\kappa g_m}\right). \tag{7}$$

Examination of (5) and (7) indicates that $C_1/C_{\rm f1}$ should be large to minimize the input-referred noise of the first stage and the noise contribution from the second stage.

C. Second-Stage Design

The schematic of the second-stage fully differential amplifier is shown in Fig. 3(a). The circuit employs capacitive feedback rather than resistive feedback to achieve low-noise operation. The midband gain A_{v2} is set by the ratio of $C_2/C_{\rm f2}$. The MOS-bipolar pseudoresistors combined with the feedback capacitors $C_{\rm f2}$ create a low-frequency high-pass corner.

The schematic of the OTA is shown in Fig. 3(b). The noise contribution from the second stage is ${v^2}_{\rm ni2}/{A^2}_{v1}$, where ${v^2}_{\rm ni2}$ represents the input-referred noise power of the second stage and A_{v1} represents the gain of the first stage. Since the noise contribution of the second stage is reduced by a factor of A_{v1}, the noise performance of the second stage can be sacrificed for ultralow-power operation. In order to reduce the flicker noise and achieve better matching, the transistors are large. The input-referred thermal noise power of the second stage can be expressed as

$$\frac{v_{\rm ni2}^2}{\Delta f} = \left(\frac{4kT}{\kappa}\frac{1}{g_{mp1}} + 16kT\gamma\frac{g_{mn1}}{g_{mp1}^2} + 8kT\gamma\frac{g_{mp6}}{g_{mp1}^2}\right)\cdot\left(\frac{C_2 + C_{f2}}{C_2}\right)^2 \tag{8}$$

where κ is the reciprocal of the subthreshold slope factor n_p and γ is the excess noise factor of the transistor in the strong inversion regime ($\gamma = 2/3$). Based on (8), the input-pair transistors $MP1$ and $MP2$ are biased in weak inversion to maximize g_m/I_D, while $MN1 - MN4$, $MP5$, and $MP6$ are biased in strong inversion regime to minimize g_m/I_D.

D. Crosstalk, Nonlinearity, and NEF

Crosstalk is an issue in a multichannel system. First, there is crosstalk from the coupling between the signal output and the input of the noncorresponding second stage. These sources of coupling can be minimized through careful layout. Second, there is crosstalk due to supply coupling. Sufficient PSRR ensures adequate rejection of the noise coupled in the supply.

The incremental resistance of the pseudoresistors is extremely high when the voltage across it is small ($|\Delta V| < 0.2$ V) [3]. However, the incremental resistance is dramatically reduced as $|\Delta V|$ increases, degrading the amplifier's linearity. Although the input transistors and the active load transistors also contribute to nonlinearity, the analysis in [9] shows that this contribution can be ignored if the amplifier has a large loop gain. Therefore, the pseudoresistors are the major cause of nonlinearity in the topology proposed in [3]. Our proposed amplifier can be expected to exhibit more nonlinearity than single-stage amplifiers (e.g., [3]–[5]), because of the larger amplitude of the second-stage input signals, but the use of two series transistors in the pseudoresistor provides sufficient linearity for the signal amplitudes expected in extracellular recording. For applications requiring greater linearity, the first-stage gain could be reduced, albeit with an increased noise contribution from the second stage. A feedback transconductor might be used in place of the pseudoresistor [7] with a modest increase in noise. If a lower high-pass corner frequency is acceptable, additional series devices can also be added to the pseudoresistor to increase the linear range.

Assuming that thermal noise is dominant and the noise of the second stage is negligible, from (5) and (7), the input-referred noise power of the amplifier is expressed as

$$\frac{v_{\rm ni}^2}{\Delta f} = \left(\frac{C_1 + C_{\rm f1}}{C_1}\right)^2 \cdot \left[\frac{4kT}{\kappa(g_{mn1} + g_{mp1})}\right]. \tag{9}$$

Since $C_1 \gg C_{\rm f1}$ and $g_{mn1} = g_{mp1} = g_m$

$$\frac{v_{\rm ni}^2}{\Delta f} \approx \frac{2kT}{\kappa g_m}. \tag{10}$$

To compare the power-noise tradeoff among amplifiers, the NEF reported in [12] is adopted

$$\text{NEF} = v_{\rm ni,rms}\sqrt{\frac{2I_{\rm tot}}{\pi \cdot U_T \cdot 4kT \cdot BW}} \tag{11}$$

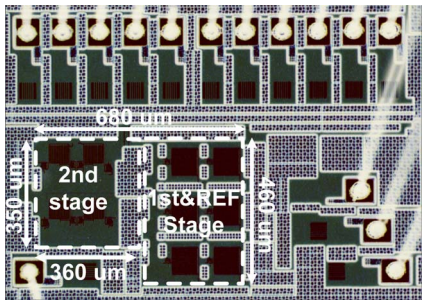

Fig. 4. Die photograph of the two-channel biopotential amplifier.

where k is the Boltzmann's constant, U_T is the thermal voltage, $v_{\mathrm{ni,rms}}$ is the total input-referred noise, BW is the -3-dB bandwidth of the amplifier, and I_{tot} is the total current consumption.

Assuming that the current consumed by the second stage is negligible ($I_{\mathrm{tot}} \approx [(N+1)/N]I_D$), the theoretical NEF limit of our proposed architecture is derived as

$$\mathrm{NEF} = \frac{1}{2\kappa} \cdot \sqrt{\frac{2(N+1)}{N}} \tag{12}$$

where $1/(2\kappa)$ is the theoretical limit of the NEF for a single-ended CRCI amplifier. By using this approach, our design can achieve a theoretical limit of NEF lower than that of a differential pair ($\sqrt{2}/\kappa$) [4]. Assuming a typical value of $\kappa = 0.7$, the NEF is equal to 1.24 for a two-channel ($N = 2$) amplifier, falling to 1.13 for $N = 8$. As the number of channels N increases, NEF gets improved due to the reduction of current consumption. Excluding the current consumption of the second stage, the proposed reference-sharing architecture allows a current reduction of $[(N-1)/2N] \times 100\%$ compared to a nonsharing configuration ($N = 1$). However, for large values of N, the complexity of a layout with good matching significantly increases, which may result in degradation of the PSRR and CMRR. In the proposed design, $N = 2$ has been selected for a reasonable tradeoff among the critical parameters, including power, NEF, and PSRR.

III. Experimental Results

We fabricated a two-channel amplifier ($N = 2$) in a 90-nm CMOS process. A die photograph is shown in Fig. 4. The total active area is 0.274 mm^2, which results in an area of 0.137 mm^2 for each channel. Each channel draws a current of 2.85 μA from a 1-V supply. Current consumption can be broken down as follows: 1.48 μA for the first stage, (1.48 μA)/2 for the reference (shared by two), and 0.63 μA for the second stage. The measured results are obtained by averaging the measured results from two channels.

The measured transfer function of the amplifier is shown in Fig. 5. The midband gain of the amplifier is 58.7 dB (34.1 dB for the first stage and 24.6 dB for the second stage). The -3-dB bandwidth is from 490 mHz to 10.5 kHz.

The input-referred noise spectrum of the amplifier is shown in Fig. 6. The total input-referred rms noise is 3.04 $\mu\mathrm{V_{rms}}$ integrated from 100 mHz to 100 kHz. By using (11) and including noise and power contributions from the second stage and the reference amplifier, our calculated NEF is 1.93. NEF can be further improved when the reference amplifier is shared by more channels. Because the conventional NEF does not consider the supply voltage, a modified metric NEF$^2 \cdot$ VDD proposed in [13] is also calculated. Our NEF$^2 \cdot$ VDD is 3.72.

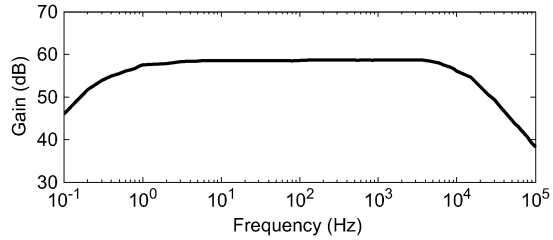

Fig. 5. Measured transfer function of the proposed amplifier.

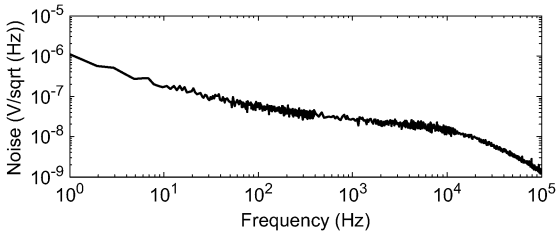

Fig. 6. Measured input-referred noise spectrum of the proposed amplifier, computed as the measured output noise spectrum divided by the midband gain.

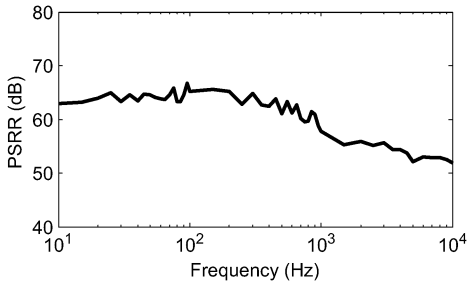

Fig. 7. Measured PSRR.

Fig. 7 shows the measured PSRR of the amplifier, which is better than 50 dB in the passband. Our amplifier is compared with a few other state-of-art neural amplifiers in Table I. Our proposed amplifier exhibits better NEF than all other amplifiers except [6], which suffers from much worse PSRR and THD. The amplifiers in [4] and [5] feature better PSRR, CMRR, and THD but have worse NEF. A smaller chip area is achieved in [7]–[10] but with inferior NEF.

Typically, low-noise regulators [14], [15] have an output rms noise $v_{\mathrm{no,reg}}$ around 20 μVrms integrated from 10 Hz to 100 kHz. The output noise of the regulator should satisfy the condition

$$v_{\mathrm{no,reg}} \ll v_{\mathrm{ni,amp}} \cdot \mathrm{PSRR}. \tag{13}$$

Assuming that the regulator noise referred to the amplifier input should be at least ten times smaller than the amplifier's own input-referred noise, an amplifier should have a PSRR better than 35 dB for typical values of $v_{\mathrm{no,reg}} = 20$ μVrms and $v_{\mathrm{ni,amp}} = 3.5$ μVrms. The PSRR (5.5 dB) of a simple single-ended amplifier [6] is not sufficient for most applications, while the improvements described in this brief yield adequate PSRR for typical application scenarios.

TABLE I
NEURAL AMPLIFIER PERFORMANCE COMPARISON

	TBioCAS 2007 [4]	JSSC 2011 [5]	EMBC 2007 [6]	TBioCAS 2012 [7]	TCASI 2013 [8]	TBioCAS 2011 [9]	TBioCAS 2007 [10]	This Work
Supply voltage (V)	2.8	2.8	1	1	1.8	1.8	1.8	1
Total current (μA)	2.7	.872	.805	12.1	6.1	4.4	4.7	2.85
Gain (dB)	40.85	39.4	36.1	40	48/60	39.4	49.5	58.7
BW (Hz)	45-5.32k	.36-1.3k	.3-4.7k	.05-10.5k	1-9k	10~7.2k	98~9.1k	.49-10.5k
$V_{ni,rms}$ (μV_{rms})	3.06	3.07	3.6	2.2	5	3.5	5.6	3.04
NEF	2.67	3.09	1.8	2.9	4.6	3.35	4.9	1.93
NEF^2Vdd	20	26.7	3.24	8.4	38.1	20.2	43.2	3.72
THD (1 mV_{pp}@1kHz)	< 1%	<1%	7.1%	1%	1.2%	<1%	<1%	1.6%
PSRR (dB)	75	>80	5.5	≥ 80	55	63.8	52	> 50
CMRR (dB)	66	>66	/	80	48	70.1	52.7	> 45*
Area (mm^2)	.16	.13	.046	.072	0.065	0.0625	0.05	.137
Process (μm)	.5	.6	.5	.13	.18	.18	.18	.09

*CMRR in Monte-Carlo simulation (100 runs).

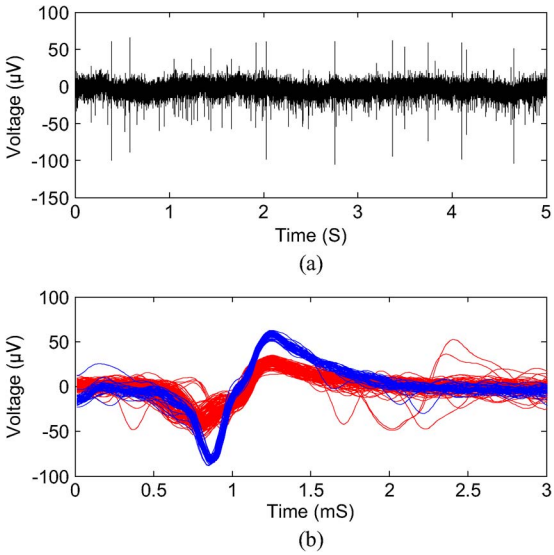

Fig. 8. Biological recordings from sensory neurons in the leg of the orange-headed cockroach *Eublaberus posticus*. (a) Long-duration trace. (b) Two classes of spikes sorted by postprocessing programs.

We verified our neural amplifier by using it to record action potentials from sensory neurons in the leg of the orange-headed cockroach *Eublaberus posticus*. A long-duration trace recorded from our amplifier, scaled by the amplifier gain, is shown in Fig. 8(a). Fig. 8(b) shows two classes of spikes recorded through the proposed amplifier, which are sorted using automated spike-sorting software [16].

IV. CONCLUSION

In this brief, we have proposed a design strategy utilizing a CRCI topology and reference-sharing architecture, which is suitable for implementing a neural recording amplifier array with ultralow-power low-noise operation. The fabricated two-channel amplifier exhibited a low input-referred noise of 3.04 μV_{rms} while consuming 2.85 μW/channel from a 1-V supply, corresponding to a NEF of 1.93. The PSRR of at least 50 dB is sufficient for typical recording scenarios. The NEF can be further improved when the reference amplifier is shared by more channels. Additionally, the 1-V supply is well suited for integration with low-power digital circuitry in complex systems-on-chip.

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