A Wideband Ultra-Low-Current On-Chip Ammeter

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Abstract—**A high-bandwidth ultra-low-current measurement circuit is presented in this paper. The circuit is capable of measuring an on-chip 50 fA current at a bandwidth up to 1 kHz with a noise floor of 0.227 $fA_{rms}/\sqrt{Hz}$. A low leakage reset scheme is utilized to improve the precision. A nested auto-zeroing scheme combined with a modified correlated double sampling is employed to mitigate the error due to various circuit imperfections. Noise analysis is carried out and "capacitive noise matching" is proposed to minimize the noise floor. The circuit is also capable of digitizing the measured current and streaming the data through a serial interface. The measurement circuit occupies 0.065 mm^2 of active silicon area in a 90nm CMOS process and consumes 147 µW from 2.5 V and 1V supplies.**

I. Introduction

High performance integrated current measurement circuits are gaining increasing research interests. They are used in interface to bionanosensors to detect ultra-low concentrations of target molecules [1], in patch-clamp recordings in electrophysiology [2], and in impedance spectroscopy of nano-scale biological or chemical samples [3]. All of the above applications require current sensing at or below the pico-ampere range with bandwidth above 1 kHz. Characterization of gate leakage currents in nanometer CMOS technologies presents another need for wide-band measurements of very small currents. As CMOS technology has progressed to ever smaller feature sizes and thinner gate oxides, gate current has become significant. Further, thin gate oxides are prone to performance degradation or catastrophic failure when subjected to prolonged stress. Previous work [4] has suggested that the presence of traps in the oxide changes the frequency spectrum of gate current noise before catastrophic oxide breakdown; so the gate current of thin-oxide transistor can be monitored to detect early signs of breakdown. To enable the characterization of gate current spectra of minimum sized transistors typically used in digital VLSI, a current level of sub-pA needs to be measured at a rate sufficient to include the frequency range in interest.

The combination of low input current and large bandwidth poses numerous design challenges. These include the leakage, charge injection and noise of the reset switch, the mismatch of components, and the large noise gain due to very small feedback capacitor used in the integrator.

In this paper we describe techniques to address these challenges and propose an on-chip ammeter (OCA) circuit. The measurement demonstrates that the circuit is able to monitor a 50 fA current at 2 kS/s sample rate. The area and power efficient design makes it suitable for multi-channel nanosensor array applications.

II. System Description

The block diagram of the proposed OCA is shown in Fig. 1. The analog part of the system is built with thick oxide IO FETs to ensure a negligible gate leakage. The front-end integrator stage converts current into a voltage ramp, the post-amplifier stage provides gain and limits noise bandwidth, and the comparator stage generates pulse signal whose width is proportional to input current. The threshold voltage of comparator is controlled by the threshold control logic to implement correlated double sampling (CDS). A 16-bit counter digitizes the pulse width; the data can then be read out through a serial interface. Dual supplies (2.5 V for analog and 1V for digital part) are used to minimize power consumption.

The integrator is realized with a 2-stage operational transconductance amplifier (OTA) with capacitive feedback. The virtual ground at the integrator input provides a constant voltage across the device under test (DUT) and eliminates the effect of parasitic capacitance on the integrator's input node, improving accuracy. To allow fast and accurate measurement of an ultra-low current, a very small integration capacitor of 30 fF and a low output swing (< 20mV) are used.

The post-amplifier stage, utilizing an OTA with capacitive feedback, amplifies the ramp signal by a factor of 20 before it is applied to the comparator. This stage suppresses the effect of the noise and offset of the comparator and limits the noise bandwidth of the system. It also acts as a buffer to isolate the integrator from kick-back noise from the comparator.

The comparator is implemented with an OTA with a switchable compensation capacitor so that it can be configured for unity gain during auto-zeroing. In normal open-loop operation, the compensation capacitor is disconnected to reduce delay. In addition, hysteresis is added to the comparator to prevent glitches and improve the noise immunity.

III. Nested Auto-zeroing and CDS Scheme

Because of the small integration capacitor and ramp height, errors due to mismatch, charge injection, and delay from each stage in this system can easily overwhelm the useful signal. Therefore, nested auto-zeroing in conjunction with a modified CDS scheme is employed to minimize these errors.

A. Nested Auto-zeroing

Each stage is coupled to the next one with a capacitor (C1 or C2 in Fig. 1). The measurement cycle starts with an auto-zeroing phase in which the reset switches S1, S3 - S5 are closed and S2 open. During this phase, the post-amplifier and comparator are configured as voltage followers; the offsets are sampled on C1 and C2 and then cancelled out in normal operation.

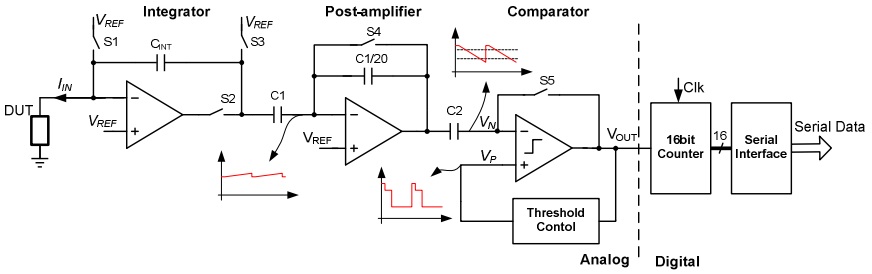


Fig. 1 System block diagram.

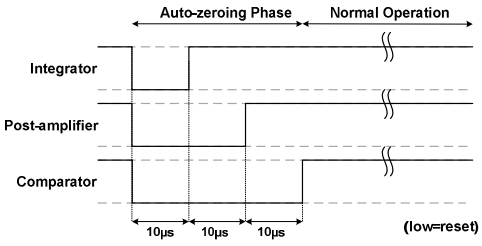


Fig.2 Timing diagram of the auto-zeroing phase.

Charge injection is another source of error. Especially at the integrator stage, a small amount of injected charge can cause a large change of the voltage across C_{INT}. The proposed nested auto-zeroing scheme uses a proper sequence of reset signals to minimize the charge injection errors. In this scheme, all the three stages enter auto-zeroing at same time. However, at the end of auto-zeroing phase, the reset switch of the first stage is released first, followed by that of the second then the third. The timing diagram is shown in Fig. 2. Charge injection due to the opening of the reset switches in the integrator stage is sampled onto C1 along with the offset of the second stage and canceled out. Charge injection due to S4 in the post-amplifier is canceled similarly. Charge injection from S5 is not canceled by auto-zeroing, but its impact is negligible because of the gain of the previous stages and the larger size of C2.

B. Modified CDS

We have also adopted a modified CDS scheme to further mitigate circuit imperfections and improve precision. Fig. 3 shows the timing diagram of the proposed scheme. V_P, V_N and V_{OUT} are the voltages at the non-inverting input, the inverting input and the output of the comparator respectively.

The proposed scheme implements CDS by applying different threshold voltages to the comparator in a sequence. In the auto-zeroing phase, the comparator is reset with a voltage of V_{CM}. At the beginning of normal operation, V_P is lowered to the first threshold Vth_{HI}. With the measured current I_{IN} discharging C_{INT} in the integrator, V_N ramps down at a rate of $20I_G/C_{INT}$. After the dead time T_D, V_N crosses the first threshold and V_{OUT} goes high, the positive edge will trigger the threshold control logic to lower V_P to the second threshold Vth_{LO}. And the current can be represented by the time (PW) between V_N crossing these two consecutive thresholds according to:

$$I_{IN} = 0.05 \cdot C_{INT} \cdot (Vth_{HI} - Vth_{LO})/PW \qquad (1)$$

Similar to conventional CDS, this scheme can reduce offset and time-correlated noise such as flicker noise. Moreover, it has several additional advantages: firstly, since the pulse width is measured between two consecutive crossings of threshold in same direction, the effect of comparator delay time is cancelled out, improving the resolution at high speed. Secondly, the freedom to tune Vth_{HI} and Vth_{LO} enables us to trade between precision and sample rate. Since the offset of the comparator has been largely removed by the auto-zeroing phase, V_{CM} can be set very close to Vth_{HI} so that the dead time T_D will not add significant overhead to the total sampling time.

IV. Integrator Design and Noise Optimization

As the system frontend, the performance of the integrator is critical because of the combined requirement of high precision and bandwidth.

A. Low Leakage Reset Scheme

The schematics and related timing diagrams of the integrator stage are shown in Fig. 4.

The integrator is built around a 2-stage OTA because it provides good noise performance, large gain, and large output swing. The switches S1-S3 are used to reset the voltage on C_{INT} at the beginning of each integration cycle. To reset, S1 and S3 are closed, while S2 is open to avoid short-circuit current. Instead of having a switch directly across C_{INT} as in [1], the proposed arrangement largely reduces the leakage current and noise of S1 because the virtual ground action of OTA will keep the voltage across S1 as small as the OTA's offset voltage. With this arrangement, the body of S1 can also be connected to V_{REF} to further reduce parasitic leakage.

At the transition from reset to integration, S1 and S3 turn off and S2 turns on. These three switches are designed to switch in a sequence as shown in Fig. 4(b) to minimize the glitches and charge injection. With the present switching sequence, only S1 generates charge injection error. S1 is implemented with a dummy switch Q_D half the size of the main switch Q_S. Q_D is driven with a delayed complementary clock signal to compensate the injected channel charge from Q_S as in Fig. 4(c).

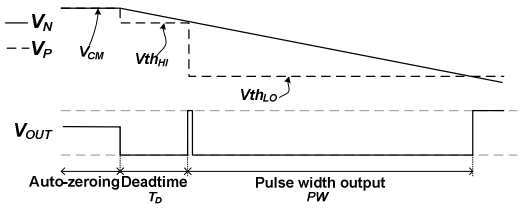


Fig. 3. Timing diagram of the proposed CDS scheme.

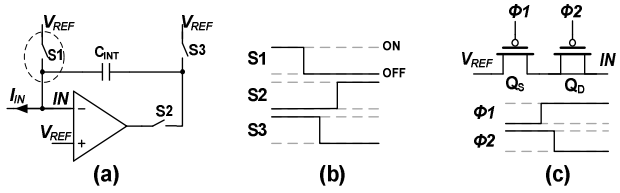


Fig. 4. (a) Schematic of integrator stage. (b) Timing diagram at the transition from reset to integration. (c) Schematic of the compensated switch S1 and its timing diagram.

B. Noise Optimization

Noise is a major factor limiting the achievable resolution, especially in the integrator. The noise gain for its input referred noise source e_n is $1+ C_P/C_{INT}$, where C_P is the parasitic capacitance at the input node. Intuitively, if e_n is dominated by the flicker noise of the input pair, it is not possible to decrease the output noise e_o arbitrarily by increasing the size, because although the input referred flicker noise decreases with the size of input pair, the C_P, thus the noise gain increases.

However, it can be shown that there exists an optimal size with which the minimum output noise is achieved. Before the derivation, two assumptions are made. Firstly, the parasitic capacitor C_P is mainly due to the C_{GS} of the OTA input pair. This is true with an on-chip DUT. Therefore,

$$C_P = \frac{1}{2}C_{GS} = \frac{1}{3}C'_{OX}WL\ ,$$

The second assumption is that is e_n is entirely due to flicker noise. In spite of the auto-zeroing and CDS, the size and the biasing of the input transistors result in a relatively high noise corner frequency. Additionally, the post-amplifier limits the system noise bandwidth to a relatively low value. These two factors combined cause the fold-over component of the flicker noise tail to dominate the input referred noise [5]. Therefore the second assumption is also valid and $e_n = \frac{A}{\sqrt{WL}}$, where A is a constant dependent on process, corner frequency, system noise bandwidth and sampling rate.

The output noise voltage is

$$e_o = e_n\left(1+\frac{C_P}{C_{INT}}\right) = \frac{A}{\sqrt{WL}}\left(1+\frac{C'_{OX}WL}{3C_{INT}}\right).$$

It can be shown that e_o takes its minimum value when

$$C_P = C_{INT}, \qquad (2)$$

And the minimum output noise is

$$e_{o,min} = 2e_n = 2A\sqrt{\frac{C'_{OX}}{3C_{INT}}}\ .$$

Next, the noise can be referred to the measured current to gain a better insight of how to optimize the noise performance. From (1), it can be shown that

$$\frac{i_n}{I_{IN}} = \frac{\Delta_{PW}}{PW} = \frac{20e_o}{Vth_{HI}-Vth_{LO}}\ ,$$

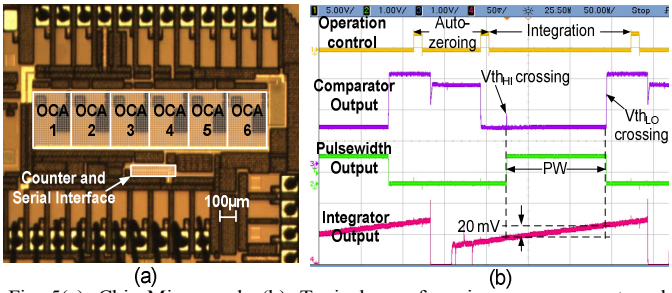
where i_n is the referred noise current, I_{IN} is the measured current, and Δ_{PW} is the jitter in output pulse width due to e_o.

Substituting $Vth_{HI} - Vth_{LO}$ using (1), we get $i_n = \frac{e_o C_{INT}}{PW}$.

Therefore, the minimum input referred current noise is achieved when condition (2) is met, and its value is

$$i_{n,min} = \frac{e_{o,min}C_{INT}}{PW} = \frac{2A}{PW}\sqrt{\frac{C'_{OX}C_{INT}}{3}}. \qquad (3)$$

Some conclusions can be drawn from the above derivation. The best noise performance is achieved when the input capacitance of the integrator is equal to the feedback capacitor, which we refer to as capacitive noise matching. Additionally, given a maximum PW (dictated by required sample rate), a smaller integration capacitor gives better noise performance. However, there is limitation for decreasing C_{INT}: if it is too small, the parasitic capacitance of the interconnection and the DUT will become significant, and the conclusions above will no longer be valid. Therefore, a balanced value of 30 fF is chosen based on layout extraction and simulation.



(a) (b)

Fig. 5(a). Chip Micrograph. (b). Typical waveform in a measurement cycle, the comparator output was distorted by the source follower buffer.

V. Mesurement Results

The proposed circuit was fabricated in a 90nm digital CMOS process and the active area is about 0.065 mm^2. The power consumption for the entire system is 146.65 µW. The die micrograph is shown in Fig. 5(a). 6 OCAs are instantiated and sharing a common counter and serial interface. Fig. 5(b) shows the typical waveform of a measurement cycle. A larger input current of 5 pA was used to make the integration ramp easier to see on the scope, the sample rate was 4 kS/s.

Fig. 6 shows the DC transfer function of the circuit, a 10 GΩ resistor is connected to the input; the voltage at the other end of the resistor is swept to generate input current. The sample rate was 2 kS/s. It can be seen that the circuit has good linearity over the range from 1 pA to 100 pA. The gain error is about 35%; it is due to the process variance of the C_{INT} and can be easily calibrated out.

Using the fabricated OCA, the gate currents of thin-oxide transistors at various conditions were characterized. Two National Instrument data acquisition cards were used to generate control signals, reference voltages and sample the output serial data.

The V-I curves of two different sized transistors are plotted in Fig. 7; the sample rate was kept at 2 kS/s. It can be shown that the presented circuit is able to measure current with a range over 3 decades (50 fA to 100 pA) with a minimum sample rate of 2 kS/s. It should be noted that this minimum sample rate limit is applied when measuring 50 fA current level, a larger sample rate can be achieved when measuring larger current (up to 10 kS/s when current is larger than 1 pA).

At the sample rate of 4 kS/s, 2 sets of gate current data of a minimum sized transistor (120nmX100nm) were acquired. The gate voltages were 1 V and 1.5 V respectively as normal and overstressed condition. Fig. 8 shows the current spectra density for each one. It can be clearly seen that the gate current spectrum of the overstressed transistor shows 1/f behavior, indicating a trapping-detrapping process in the oxide due to the large applied field. This result also gives an upper bound of the measurement circuit noise floor of 0.8 $fA_{rms}/\sqrt{Hz}$.

In Fig. 9 the measured current noise is compared to the shot noise model to get a better estimate of the noise floor. The gate current noise can be modeled as shot noise because the current comprises individual electrons tunneling though gate oxide at random intervals. The noise bandwidth of the measurement circuit was kept at 2 kHz in this measurement by varying the thresholds to maintain a constant integration time.

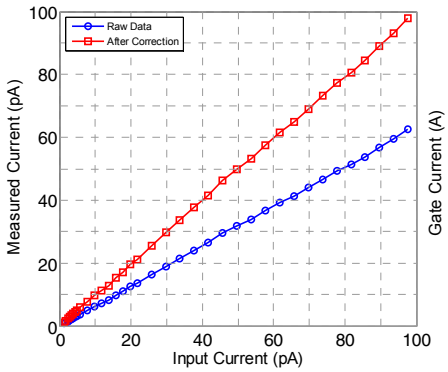


Fig. 6. DC transfer function, the raw data was processed to correct for the gain error.

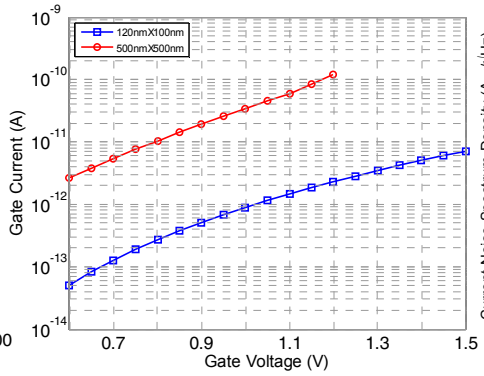


Fig. 7. Gate current versus gate voltage of two different sized transistors.

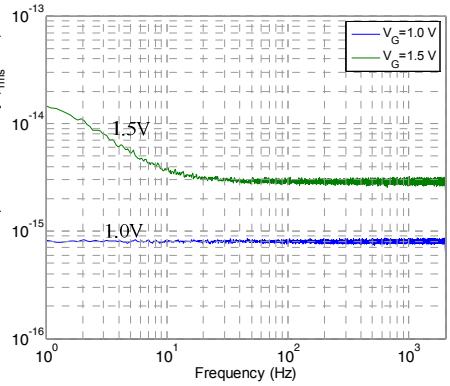


Fig. 8. Noise Spectrum of a transistor under normal and overstressed conditions.

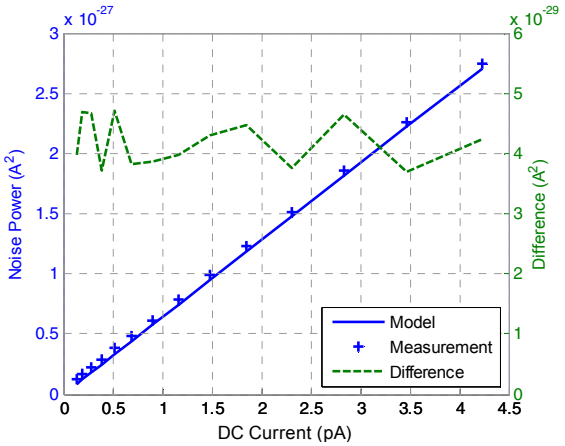


Fig. 9. Comparison of shot noise model and the measured current noise, the difference is constant and can be used to estimate the circuit noise floor.

The measured value agrees well with the model, the difference in noise power between the measurement and model is nearly constant and can be attributed to the measurement circuit noise. Therefore, the noise floor can be determined to be less than 7 fA_{rms} over 2 kHz bandwidth. It should be noted that the 2 kHz bandwidth refers to the bandwidth of the 250 µs integration window. The actual sampling period is 340 µs including the overhead time. Applying the correction factor from the measurement shown in Fig. 6, we estimate an input-refered noise floor of 0.227 $fA_{rms}/\sqrt{Hz}$.

In Table I, the measured performance is summarized and compared to several recently reported low current measurement system. The proposed OCA is capable of measuring lower current at higher bandwidth and has good overall performance in terms of noise, power and area.

TABLE I
PERFORMANCE SUMMARY AND COMPARISON

	This Work	ISSCC '09 [1]	JSSC '09 [3]	TBioCA S'12 [6]
Technology	**90nm CMOS**	0.35µm CMOS	0.35µm CMOS	0.5um CMOS
Supply	**2.5V/1V**	3.3V	±1.5V	3.3V
Structure	**Integrator**	Integrator	Trans-impedance	Integrator
Bandwidth @ input current†	**1 kHz @ 50 fA**	1 kHz @ pAs	4 MHz	5 kHz @ 10 pA
Noise Floor ($fA_{rms}/\sqrt{Hz}$)	**0.227***	4.74	4	6*
Area (mm^2)	**0.065**	0.5	0.34	0.14
Power (mW)	**0.147**	23	45	1.5

† The sample rates at lower end of input range are recorded
* Achieved with on-chip measurement

VI. CONCLUSIONS

We have presented a high-bandwidth ultra-low-current on-chip ammeter. By employing several novel circuit techniques including a three-stage design, low leakage reset scheme, nested auto-zeroing and modified CDS, the circuit is made robust against leakage, mismatch and charge injection. Capacitive noise matching methodology is derived and utilized to minimize the noise floor of the capacitive feedback integrator. The circuit occupies 0.065 mm^2 of active area and is able to measure a 50 fA on-chip current at 2 kS/s sample rate with a noise floor of 0.227 $fA_{rms}/\sqrt{Hz}$, and a power consumption of 147 µW.

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