

# A Low-Power 84-dB Dynamic-Range Tunable Gm-C Filter for Bio-Signal Acquisition

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**Abstract**—A tunable Gm-C filter is presented for bio-signal acquisition application. It incorporates linear tunable transconductors utilizing MOSFETs biased in the triode region. Both the filter architecture and transconductor circuit design are optimized for good tuning, linearity and noise performance with low power consumption. The filter was fabricated in a 0.6  $\mu\text{m}$  BiCMOS process, occupying 0.17  $\text{mm}^2$ . Measurement results show a tuning range of cut-off frequency from 2.5 kHz to 10 kHz. At 5 kHz cut-off frequency, the filter achieves a dynamic range of 85 dB with 1% THD, and consumes 75.9  $\mu\text{W}$  from 3.3 V supply.

**Keywords**— Gm-C filter, transconductor, bio-signal acquisition

## I. INTRODUCTION

Bio-potential signals provide vital information about the patient for disease diagnosis and health monitoring. Fig. 1 shows the block diagram of a typical bio-signal acquisition system. In the analog frontend, the ac-coupled low-noise amplifier (LNA) and the programmable-gain amplifier (PGA) provides gain to reduce noise contribution of subsequent blocks [1] [2]. They are followed by a low-pass filter to eliminate the out-of-band noise. In addition, this filter acts as anti-aliasing filter for the ADC backend. In biomedical applications, it is often desirable to have a filter with tunable cut-off frequency as the bio-signal can range from sub-Hz to a few kHz [3]. In a wearable or implantable system, low power consumption is imperative to extend the battery life and avoid heating of nearby tissue. Furthermore, as the bio-signal amplitude can range from several microvolts to tens of millivolts, high dynamic range (high linearity with low noise) is required to maintain fidelity of the acquired signal. All these requirements place challenges on the filter design.

The filter function can be integrated in the LNA by adding load capacitors at the output of the amplifier [4]. This approach is not economic in terms of chip area because the LNA is normally placed in a feedback loop and has large transconductance ( $g_m$ ), resulting in a large load capacitor value for low corner frequency. Switch-capacitor circuits are used to implement the filter in [5]. However, this sampled-data system has the potential problem of out-of-band interference and noise being folded back to baseband by aliasing. Active RC filters show good linearity performance due to the virtual ground provided by the op-amp, but they normally do not have continuous tuning capability and rely on the availability of high quality resistors in the process. Another popular type of filter is the Gm-C filters [6]. They are built with transconductors and capacitors. The frequency tuning is easily achieved by varying the  $g_m$  of the transconductor, and the absence of feedback allows them to have better frequency response than active RC filters.

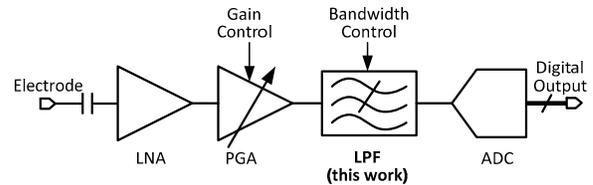


Fig. 1. Block diagram of a typical bio-signal acquisition system.

The performance of the Gm-C filter is largely determined by the transconductor, as it is the only active component and operates in open-loop configuration.

In this paper, a second-order Gm-C filter for bio-signal acquisition application is presented. The filter incorporates linear tunable pseudo-differential transconductors, which are based on transistors biased in the triode region. A common-mode feedback (CMFB) circuit maintains suppression of CM component across the entire range of output swing. Both the architecture and circuit design are optimized specifically for bio-signal acquisition application with wide tuning range, high dynamic range and low power consumption.

## II. TRANSCONDUCTOR CELL DESIGN

### A. Triode Transconductor

In a Gm-C filter, the transconductors are required to have good linearity with large differential signal input, and tunable transconductance. Common linearization techniques include source degeneration [7], bias offset [8] and source coupling [9]. The tunability can be achieved by tunable active resistor [7] [10], or current division [11]. Apart from these techniques, transconductors based on transistors biased in the triode region are good candidates as they show good linearity and wide tuning range with low circuit complexity.

For a transistor biased in the triode region, its drain current is given by

$$I_D = \mu C_{OX} \frac{W}{L} V_{DS} (V_{GS} - V_{TH} - \frac{V_{DS}}{2}), \quad (1)$$

where  $\mu$  is the mobility,  $C_{OX}$  is the unit gate capacitance and  $V_{TH}$  is the threshold voltage. The transconductance is then obtained by taking derivative of  $I_D$  with respect to  $V_{GS}$

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = \mu C_{OX} \frac{W}{L} V_{DS}, \quad (2)$$

indicating that  $g_m$  is independent of  $V_{GS}$ , and tunable by  $V_{DS}$ .

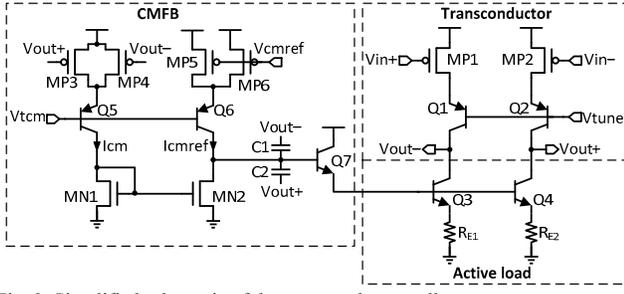


Fig. 2. Simplified schematic of the transconductor cell.

### B. Overall Design

The simplified schematic of the transconductor is shown in Fig. 2. MP1/MP2 is the input transistor biased in the triode region by the cascode transistor Q1/Q2 [12].  $V_{tune}$  determines the  $V_{DS}$  of MP1/MP2 and therefore the  $g_m$  of the trans-conductor. The upper boundary of  $V_{tune}$  is limited by the  $V_{BE}$  mismatch of Q1/Q2, which becomes significant when  $|V_{DS}|$  of MP1/MP2 gets lower, while the lower boundary is limited by the linearity: as  $V_{tune}$  is reduced, MP1/MP2 begins to transition out of the triode region. Transistor Q3/Q4 and degeneration resistor  $R_{E1,2}$  act as active load, whose current is controlled by the CMFB circuit.

The design of CMFB circuit in a linear transconductor is not trivial, as the CM path needs to be as linear as the differential mode (DM) one to maintain good suppression of CM component and interference. The commonly used CMFB circuit using differential pairs [13] is not adequate in this application because the large differential swing at the output can completely turn off one input transistor and cause non-linearity. The proposed CMFB circuit uses a structure similar to the DM path and therefore offers comparable linearity. Triode transistors MP3/MP4 convert the output voltages to CM currents  $I_{cm}$ .  $I_{cm}$  is then mirrored by MN1/MN2 and compared to  $I_{cmref}$ , which is a current generated from the CM reference voltage  $V_{cmref}$  by MP5/MP6. MP3-6 have the same aspect ratio, so the negative feedback loop stabilizes the CM output to  $V_{cmref}$ . Q7 compensates for the base current of Q3/Q4. Capacitor C1/C2 provides frequency compensation to ensure the stability of the loop. It's worth noting that C1/C2 at the same time serves as the load capacitance for the filter therefore does not consume significant area overhead.

### C. Linearity, Noise and Power Considerations

Equation (2) suggests ideally linear transconductance of the triode transistor. However, second-order effects such as mobility degradation due to vertical field degrade the linearity by making the mobility input-dependent:

$$\mu = \frac{\mu_0}{1 + \theta(V_{GS} - V_T)}, \quad (3)$$

where  $\mu_0$  is the mobility without degradation, and  $\theta$  is the mobility degradation factor. The employment of fully differential structure largely mitigates this nonlinearity as the first-order components cancel each other.

The other assumption in (2) is that the  $V_{DS}$  of the input transistors are kept constant, regardless of input. This can be achieved by adoption of regulated-cascode technique in which

an amplifier provides negative feedback to fix the drain voltage of the input transistor [14]. This amplifier, however, adds extra area and power consumption. Moreover, the noise of the amplifier contributes significantly to the output noise because the low drain resistance of the input transistor is insufficient to attenuate the cascode transistor and amplifier's input-referred noise. Instead, we take the advantage of the BiCMOS process and use bipolar transistors as cascode devices. As the  $g_m$  of the cascode devices Q1/Q2 is much larger than that of the input device MP1/MP2, the  $V_{DS}$  variation can be greatly reduced to the point that its effect on the non-linearity is insignificant.

The amplitude of bio-signals can be as low as several microvolts. Therefore the noise floor of the acquisition system needs to be low enough to maintain acceptable signal to noise ratio (SNR). In the frequency band of interest (10 Hz-10 kHz), the dominant noise source is the flicker noise in MOSFETs. Therefore, we extensively use bipolar transistors to eliminate this noise. For the input devices, PMOSs are used because they show much lower flicker noise than NMOSs in this process. In addition, to minimize the noise contribution of the active load, emitter degeneration is employed. Proper design ensures that the noise in the active load is dominated by the resistor  $R_E$ , and the input referred noise power is given by:

$$V_{n,in}^2 = V_{n,p}^2 + \left( \frac{1}{g_{m,p}} \right)^2 \left( V_{n,cas}^2 g_{ds,p}^2 + \frac{4KT}{R_E} \right), \quad (4)$$

where  $V_{n,p}^2$ ,  $g_{m,p}$  and  $g_{ds,p}$  are the input referred noise, transconductance (given by (2)) and drain conductance of the input device MP1/MP2, respectively,  $V_{n,cas}^2$  is the input referred noise of the cascode device Q1/Q2,  $K$  is the Boltzmann constant and  $T$  is the temperature in Kelvin. Assuming that  $|V_{DS}|$  is small enough that the channel is homogeneous (when  $V_{tune}$  is high enough),  $V_{n,p}^2$  can be expressed as

$$V_{n,p}^2 = \frac{4KT}{g_{m,p}} \left( \frac{V_{GS} - V_{TH}}{V_{DS}} \right) + \frac{K_F}{C_{OX}WLf}, \quad (5)$$

where  $K_F$  is the flicker noise coefficient. The input referred noise of the cascode bipolar transistor is given by

$$V_{n,cas}^2 = 4KT r_b + 2qI_B r_b^2 + 2qI_C \left( \frac{r_b}{\beta} + \frac{U_T}{I_C} \right), \quad (6)$$

where  $r_b$  is the base spread resistor, and  $U_T$  is the thermal voltage. Equations (4)-(6) indicate direct trade-offs between noise and power/area: as we increase  $g_{m,p}$  to reduce noise, power consumption increases and the filter capacitance also has to increase to maintain the same corner frequency. Therefore, we performed optimization to meet the system dynamic range and SNR requirement, while keeping the power and area to their minimum. The noise on the bias voltages ( $V_{tune}$ ,  $V_{cmref}$ ,  $V_{tcm}$ ) only contributes to the common-mode noise therefore has negligible effect on the filter performance.

### III. FILTER DESIGN

The proposed transconductor cell is used to implement a second-order low-pass filter. The filter design adopts the biquad

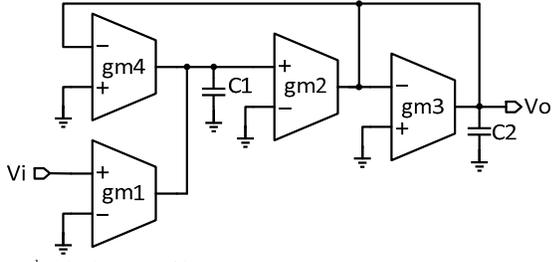


Fig. 3. 2<sup>nd</sup> order low-pass filter structure.

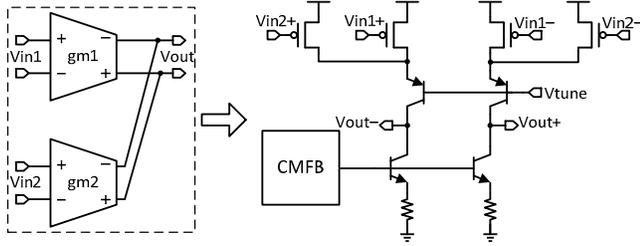


Fig. 4. Combination of two transconductors to share the load and CMFB.

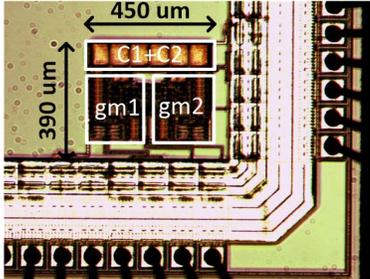


Fig. 5. Chip micrograph of the proposed filter.

structure [6] and its schematic is shown in Fig. 3. It can be shown that the filter has a transfer function of

$$H(s) = \frac{Vo(s)}{Vi(s)} = \frac{\frac{g_{m1}g_{m2}}{C_1C_2}}{s^2 + s\frac{g_{m3}}{C_2} + \frac{g_{m2}g_{m4}}{C_1C_2}}. \quad (7)$$

We choose  $g_{m1-4} = g_m$  to facilitate matching. The filter's cut-off frequency ( $f_c$ ) and quality factor ( $Q$ ) are given by [6]:

$$f_c = \frac{g_m}{2\pi\sqrt{C_1C_2}}, \quad (8)$$

$$Q = \sqrt{\frac{C_2}{C_1}}.$$

Note that  $Q$  is determined by the capacitor ratio therefore can be very accurate. To get a maximal flatness in the passband, Butterworth type is chosen and  $Q = 0.707$ .  $f_c$  is tunable by varying  $g_m$ , while  $Q$  is unaffected by this tuning.

As shown in Fig. 3,  $g_{m1}$  and  $g_{m4}$  share the same output nodes, so does  $g_{m2}$  and  $g_{m3}$ . Therefore, each pair can share their cascode

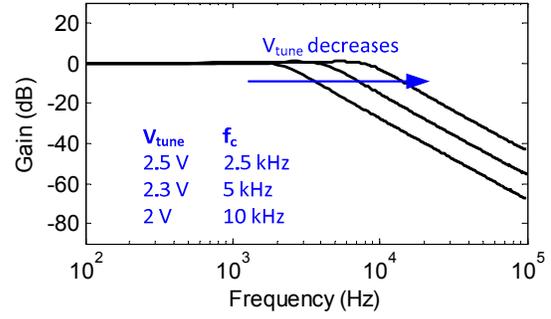


Fig. 6. Measured frequency response of the filter, showing tunable cut-off frequency  $f_c$  by  $V_{tune}$ .

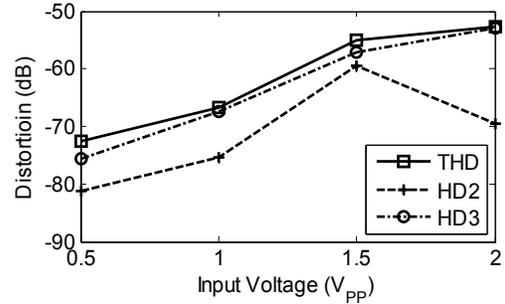


Fig. 7. Measured THD, HD2 and HD3 at 5 kHz  $f_c$  with 1 kHz sine wave input as a function of input peak-to-peak voltage.

transistors, active loads and CMFB circuits, significantly reducing the area and power consumption of the filter system. Fig. 4 shows how two transconductors can be combined to a single transconductor with two inputs.

#### IV. MEASUREMENT RESULTS

The second-order Butterworth low-pass filter is fabricated in a 0.6  $\mu\text{m}$  BiCMOS process to facilitate low-noise design of the filter as well as the LNA, occupying 0.17  $\text{mm}^2$  active area, shown in Fig. 5. The supply voltage is 3.3 V.

The measured frequency response magnitude is shown in Fig. 6, showing a tunable cut-off frequency from 2.5 kHz to 10 kHz when the tuning voltage  $V_{tune}$  varied from 2.5 V to 2 V. The filter power consumption also varies with the tuning as listed in Table I.

The linearity of the filter is measured with 1 kHz sine wave. The total harmonic distortion (THD), second order (HD2) and third order (HD3) harmonic distortions at the output are plotted in Fig. 7 with 5 kHz  $f_c$  as a function of differential input peak-to-peak voltage. It can be seen that the THD is below  $-66$  dB with 1  $V_{pp}$  input. The differential input to generate a 1% THD is about 4  $V_{pp}$ , verifying good linearity of the transconductor, and the CMFB circuit. Similar measurement results with other cut-off frequency values are listed in Table I.

The output noise spectrum with 5 kHz  $f_c$  is shown in Fig. 8. The flicker noise from the input transistors is the major contributor in the frequency band of interest and the integrated output noise from 10 Hz to 100 kHz is measured to be 78.2  $\mu\text{V}_{rms}$ . The noise at frequencies above 100 kHz is strongly reduced by

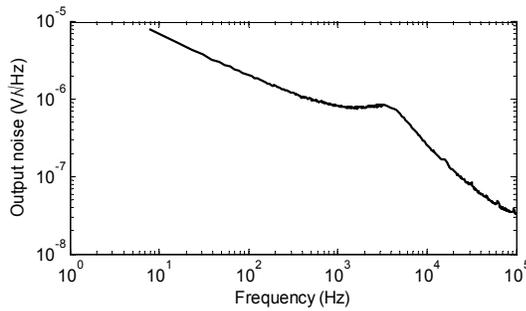


Fig. 8. Output noise spectrum with 5 kHz cut-off frequency.

TABLE I. PERFORMANCE SUMMARY OF THE FILTER

Technology	0.6 $\mu\text{m}$ BiCMOS		
Area	0.17 $\text{mm}^2$		
Supply (V)	3.3 V		
Corner Frequency	2.5kHz	5kHz	10kHz
Power ( $\mu\text{W}$ )	47.2	75.9	111.2
THD @ $V_{in}=1V_{pp}$ (dB)	-69.79	-66.69	-60.54
Input $V_{pp}$ @ 1% THD (V)	4.13	3.94	3.13
Noise 10Hz-100kHz ( $\mu\text{V}_{rms}$ )	91.8	77.3	60.7
Dynamic Range (dB)	84.03	85.13	85.23

TABLE II. PERFORMANCE COMPARISON

	This work	[16]	[17]	[18]
Supply (V)	<b>3.3</b>	1.5	1.8	1.8
Technology	<b>0.6 <math>\mu\text{m}</math></b>	0.18 $\mu\text{m}$	0.18 $\mu\text{m}$	0.18 $\mu\text{m}$
Area ( $\text{mm}^2$ )	<b>0.17</b>	0.11	0.3	0.16
Power ( $\mu\text{W}$ )	<b>75.9</b>	240	800	4070
Tuning Range (Hz)	<b>2.5k-10k</b>	20k-86k	250-1M	462k-2.61M
Dynamic Range @ 1% THD (dB)	<b>85</b>	75	48	45
FOM (aJ)	<b>33.73</b>	71.56	456.9	20531

the filter's attenuation. The dynamic range is 85 dB with 1% THD, well-suited for bio-signal acquisition applications. From Table I, it can be seen that the dynamic range is above 84 dB across the entire tuning range.

In Table I, the performance of the filter at different values of  $f_c$  is summarized. The performance with  $f_c=5$  kHz is compared to similar previous works in Table II. In order to compare the performance of different implementations, we use the figure-of-merit in [15]:

$$FOM = \frac{P_{diss}}{pQ_{max}f_cDR^2}, \quad (9)$$

where  $P_{diss}$  is the power dissipation,  $p$  is the number of filter poles,  $f_c$  is the cut-off frequency, and  $DR$  is the dynamic range of the filter. A lower FOM indicates a more power-efficient design. It can be seen that the proposed filter achieves the best dynamic range with lower power consumption, and the best FOM in the comparison.

## V. CONCLUSIONS

We present a Gm-C low pass filter utilizing tunable linear transconductors based on triode transistors. The system architecture and circuit are designed to achieve both low power

and high dynamic range. The measurements of the filter show 2 octaves tuning range of cut-off frequency, and a dynamic range of 85 dB with 75.9  $\mu\text{W}$  power consumption. The performance compares favorably with previous works, and the system is well-suited for bio-signal acquisition applications.

## REFERENCES

- [1] T. Yang, J. Lu and J. Holleman, "A high input impedance low-noise instrumentation amplifier with JFET input," in *Proc. IEEE Int. Midwest Symp. Circuits and Syst. (MWSCAS)*, Aug. 2013, pp. 173-176.
- [2] T. Yang, J. Lu, N. Poore and J. Holleman, "A current-reuse complementary-input chopper-stabilized amplifier for neural recording," in *Proc. IEEE NEWCAS*, Jun. 2014.
- [3] X. Zou, X. Xu, L. Yao and Y. Lian, "A 1-V 450-nW fully integrated programmable biomedical sensor interface chip," *IEEE J. Solid-State Circuits*, vol. 44, no. 4, pp. 1067-1077, Apr. 2009.
- [4] Q. Li, K. H. R. Tan, T. T. Hui and R. Singh, "A 1-V 36- $\mu\text{W}$  low-noise adaptive interface IC for portable biomedical applications," in *Proc. European Solid State Circuits Conf. (ESSCIRC)*, Sept. 2007, pp. 288-291.
- [5] L. Lentola, A. Mozzi, A. Neviani and A. Baschiroto, "A 1- $\mu\text{A}$  front end for pacemaker atrial sensing channels with early sensing capability," *IEEE Trans. Circuits and Syst. II: Analog and Digit. Sig. Process.*, vol. 50, no. 8, pp. 397-403, Aug. 2003.
- [6] R. Geiger and E. Sanchez-Sinencio, "Active filter design using operational transconductance amplifiers: A tutorial," *IEEE Circuits and Devices Mag.*, vol. 1, no. 2, pp. 20-32, Mar. 1985.
- [7] J. Lu, T. Yang, M. S. Jahan, and J. Holleman, "A nano-power tunable bump circuit using a wide-input-range pseudo-differential transconductor," *Electron. Lett.*, vol. 50, no. 13, June. 2014.
- [8] Z. Wang and W. Guggenbuhl, "A voltage-controllable linear MOS transconductor using bias offset technique," *IEEE J. Solid-State Circuits*, vol. 25, no. 1, pp. 315-317, Feb. 1990.
- [9] A. Nedungadi and T. R. Viswanathan, "Design of linear CMOS transconductance elements," *IEEE Trans. Circuits Syst.*, vol. 31, no. 10, pp. 891-894, Oct. 1984.
- [10] C. Luján-Martínez, R. Carvajal, J. Galán, A. Torralba, J. Ramirez-Angulo and A. López-Martín, "A tunable pseudo-differential OTA With -78dB THD consuming 1.25 mW," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 55, no. 6, pp. 527-531, Jun. 2008.
- [11] J.-Y. Lee, C.-C. Tu and W.-H. Chen, "A 3 V linear input range tunable CMOS transconductor and its application to a 3.3 V 1.1 MHz Chebyshev low-pass Gm-C filter for ADSL," in *Proc. IEEE Custom Integr. Circuit Conf.*, May 2000, pp. 387-390.
- [12] R. Alini, A. Baschiroto and R. Castello, "Tunable BiCMOS continuous-time filter for high-frequency applications," *IEEE J. Solid-State Circuits*, vol. 27, no. 12, pp. 1905-1915, Dec. 1992.
- [13] J. Galán, M. Pedro, C. Rubia-Marcos, R. Carvajal, C. Luján-Martínez and A. López-Martín, "A low-voltage, high linear programmable triode transconductor," in *Proc. IEEE Int. Symp. Circuits and Syst. (ISCAS)*, May 2010, pp. 221-224.
- [14] P. Likittanapong, A. Worapishet and C. Toumazou, "Linear CMOS triode transconductor for low-voltage applications," *Electron. Lett.*, vol. 34, no. 12, pp. 1224-1225, Jun. 1998.
- [15] T. Laxminidhi, V. Prasadu and S. Pavan, "Widely programmable high-frequency active RC filters in CMOS technology," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 56, no. 2, pp. 327-336, Feb. 2009.
- [16] U. Yodprasit and C. Enz, "A 1.5-V 75-dB dynamic range third-order Gm-C filter integrated in a 0.18- $\mu\text{m}$  standard digital CMOS process," *IEEE J. Solid-State Circuits*, vol. 38, no. 7, pp. 1189-1197, Jul. 2003.
- [17] T.-Y. Lo and C.-C. Hung, "A wide tuning range Gm-C continuous-time analog filter," *IEEE Trans. Circuits Syst. I: Reg. Papers*, vol. 54, no. 4, pp. 713-722, Apr. 2007.
- [18] X. Zhang and E. El-Masry, "A novel CMOS OTA based on body-driven MOSFETs and its applications in OTA-C filters," *IEEE Trans. Circuits Syst. I: Reg. Papers*, vol. 54, no. 6, pp. 1204-1212, Jun. 2007.