A 3.3 µW Dual-Modulus Frequency Divider with 189% Locking Range for MICS Band Applications

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Abstract— **This paper presents the design and simulated performance of an ultra-low-power 4/5 frequency divider based on a CMOS ring oscillator. The divider operates over a 189% locking range (29MHz – 1GHz) for both division ratios, covering the MICS band and 433MHz and 915MHz ISM bands while consuming only 3.3 µW in MICS band. The wide locking range and low power consumption makes this very suitable for ultra-low-power MICS band applications. The divider is designed in 90 nm CMOS process and occupies 45 µm^2 area.**

I. Introduction

The need for highly integrable and low-power frequency synthesizers for implantable and body-worn wireless medical devices is continuously growing. In any phase-locked loop frequency synthesizer, the voltage-controlled oscillator and the frequency divider typically dominate power consumption, since they run at full RF frequency. Power consumption of high-frequency divider blocks can be reduced, using a low-power divider as a pre-scaler to reduce the operating frequency for the subsequent digital dividers.

Two common topologies for low-power pre-scalers are dynamic logic dividers and Injection-Locked Frequency Dividers (ILFD). Dynamic logic dividers can provide very large locking range, but with relatively high power consumption [1]. ILFDs, on the other hand, can operate at very low power, being based on low-frequency oscillators, but generally suffer from limited locking range [2] – [6].

In this paper, we describe a dual-modulus divider and present detailed design considerations for maximizing frequency range and minimizing power consumption. The proposed divider combines features from dynamic logic dividers and injection-locked dividers, in a topology similar to that in [7], to simultaneously achieve wide locking range and low power consumption. The designed divider in this work shows a locking range from 29 MHz to 1 GHz (189%) covering the 402-405 MHz MICS band and 433 MHz and 915 MHz ISM bands while consuming only 244 nW to 8.5 µW across the frequency range from a 1 V supply. The divider is designed in 90 nm CMOS process. Post-layout simulation results across a wide range of temperature and process conditions are provided.

II. Design Implementation

The frequency divider designed in this work is based on a 5-stage ring oscillator. The divider consists of 5 clocked inverters with PMOS headers and NMOS footers. The divider also has an extra parallel header in one stage to function as a modulus-control (MC) switch. The divider is designed in a 90 nm CMOS process with minimum size transistors (W = 120 nm, L = 100 nm) to ensure minimum load capacitance for each stage and thus, minimize power consumption. Fig. 1 shows the structure of the divider.

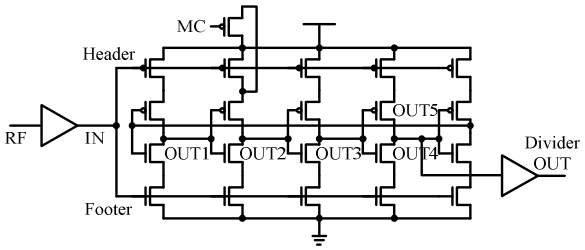

Fig. 1. Schematic of the proposed ÷4/÷5 frequency divider.

A. Operation of Divider

The key factor in the operation of the developed divider is controlled propagation of the oscillation signal through the stages of the oscillator [7]. When MC switch is turned off (MC = logic '1'), the proposed divider is in divide-by-5 mode, and MC switch is turned on (MC = logic '0'), the divider is in divide-by-4 mode. Figs. 2 and 3 illustrate the operation of this divider.

In ÷5 mode, the transitions in the outputs of all inverter stages are controlled by the digital input signal (IN) through corresponding headers and footers. For example, if OUT1 becomes logic low, OUT2 has to wait for the following "low" half-cycle of IN signal, so that the header of the second stage turns on, allowing OUT2 to rise. In this way, five stages require five consecutive IN half-cycles for a transition in an OUT signal to propagate through the five stages. Therefore, a cycle in any OUT signal consists of five IN cycles and thus, divide-by-5 operation occurs.

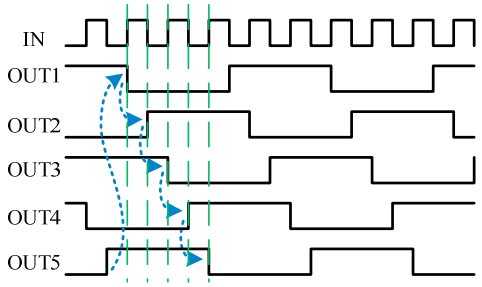

Fig. 2. Divide-by-5 operation of the designed divider (MC = logic '1'). The blue arrows indicate propagated transitions controlled by input signal.

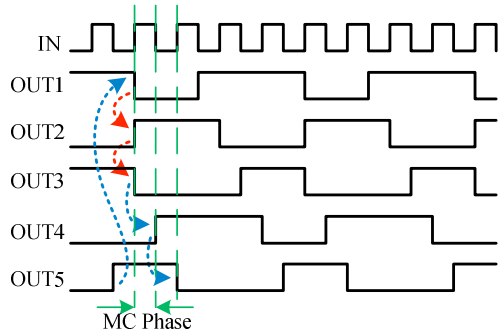

Fig. 3. Divide-by-4 operation by the deigned divider (MC = logic '0'). The red arrows indicate the "pulse swallowing" phenomenon in MC phase.

In ÷4 mode, illustrated in Fig. 3, the second stage has a parallel header (MC) that is always turned on. As a result, when OUT1 becomes low in a "high" IN half-cycle, which we will refer to as "Modulus-Control phase" or "MC phase", OUT2 becomes high, allowing OUT3 to become low in the same IN half-cycle, instead of the next "high" IN half-cycle. In the process, an IN cycle is thus "swallowed" and an OUT cycle corresponds to four IN cycles. Thus, in this case, the frequency divider performs a divide-by-4 operation.

B. Design Considerations

Two 2-stage buffers have been used at the input (IN) and output (OUT4) nodes of the divider. The input buffer is configured so that the input signal to the divider IN has more than 50% duty cycle. This is to allow more time in the "MC phase" to easily accommodate three OUT edges in ÷4 mode. Figs. 4 and 5 show the proposed divider's divide-by-5 and divide-by-4 operations respectively at 400 MHz input frequency and room temperature (27°C). Some glitches can be seen in the OUT signals due to feedback and feed-forward of the signals through gate-drain capacitances.

Simulations have been performed at temperature and process extremes to identify limitations on the proposed divider's performance. The edge-time of the OUT signals sets limit for high-frequency and low-temperature operation of the divider, whereas leakage through the transistors limit its low-frequency and high-temperature operation. In this section, we discuss factors that limit functionality in the extremes of the divider's frequency range and design techniques to address such factors.

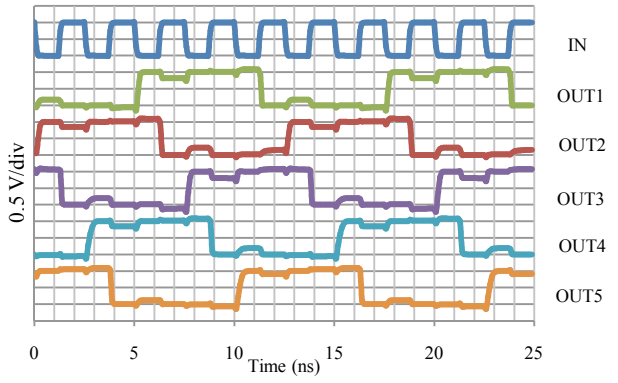

Fig. 4. Post-layout simulation of divide-by-5 operation of the proposed divider at 400 MHz input frequency and 27°C temperature.

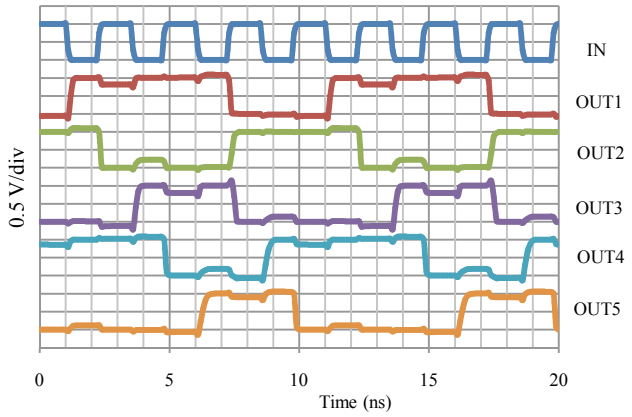

Fig. 5. Post-layout simulation of divide-by-4 operation of the proposed divider at 400 MHz input frequency and 27°C temperature.

1) PMOS MC Switch: In [7], an NMOS has been used as the modulus-control switch. Therefore, in that divider, in ÷4 mode, the "MC phase" consists of rising edges of two OUT signals and one falling edge of another (the stage with the MC switch).Since, in this work, both the PMOS and NMOSs are chosen as minimum-size to reduce power consumption, the rising edges are slower than the falling edges. This limits the divider's ÷4 operation at high-frequency or low-temperature extreme, as the pulse-width of input signal must be wide enough to accommodate these three edges. Therefore, a PMOS is used as the MC switch of the proposed divider. In this case, the MC phase consists of two falling edges (faster) and one rising edge (slower) and thus, is allowed to be narrower. A wider PMOS (W = 300 nm) has been used for the MC switch to narrow the rising edge in the MC phase. Fig. 6 shows a post-layout simulated (slow-slow corner) view of the MC phase at the proposed divider's ÷4 operation at 1.026 GHz and -40°C, the limit of the divider's functionality at high-frequency-low-temperature range. It can be seen that the "high" half-cycle of the input signal is just wide enough to accommodate the three edges of OUT signals for a successful divide-by-4 operation.

It is to be noted that the rise-time of OUT5 is a limiting factor for high-frequency operation. In layout, the OUT5 node needs longer routing than nodes OUT1 – OUT4 to connect the output of the fifth stage and the input of the first stage. Hence, OUT5 has more parasitic capacitance than OUT1 – OUT4 and its edge-times are longer than others', limiting high frequency operation. The output buffer is therefore driven from OUT4 rather than OUT5 to evenly distribute excess capacitance and thus avoid reduction of the frequency range.

2) Modification of the Stage following the MC-Switched Stage: Fig. 7 shows a detailed view of the second and third stages along with the modification in the third stage of the proposed divider. At the low-frequency, high-temperature extreme, the divider's functionality is limited by transistor leakage. Particularly, a specific glitch in OUT2 signal causes extra leakage in the third stage. The waveforms of OUT1 – OUT3 are shown in Fig. 8.

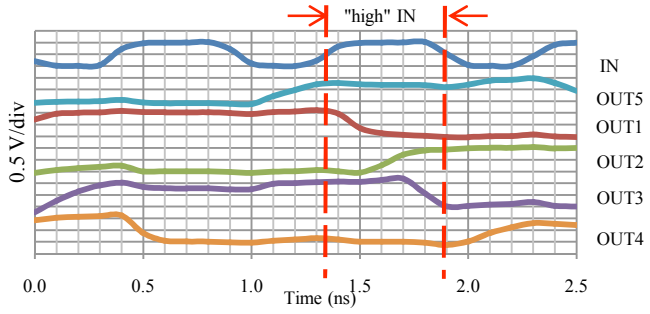

Fig. 6. Post-layout simulation of ÷4 operation (slow-slow corner) at 1.026 GHz and -40°C operating temperature. The "high" half-cycle of IN (input signal) is just wide enough to accommodate the three edges of OUT signals in one "MC phase".

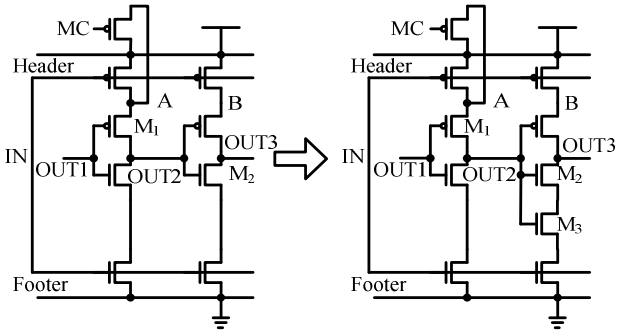

Fig. 7. Detailed schematic view of second and third stages of the divider. In the third stage, NMOS M_3 is added in series with M_2 to reduce leakage from OUT3 resulting from the effect of large parasitic capacitance in node A.

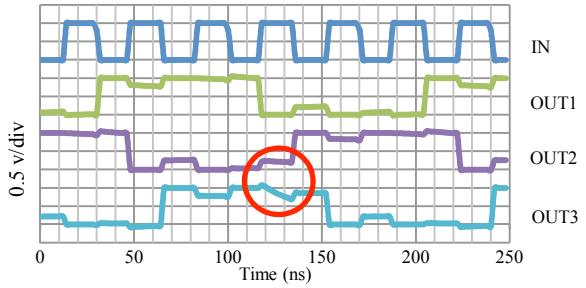

Fig. 8. Post-layout simulation of ÷5 operation (fast-fast corner) at 28.57 MHz and 125°C. A noticeable decay in 'high' OUT3 is due to leakage through NMOS in the third stage that happens as a result of the rise in OUT2. The leakage is reduced by adding an extra NMOS, M_3, in series in the third stage. This phenomenon is observed in other OUT signals, but in less amount.

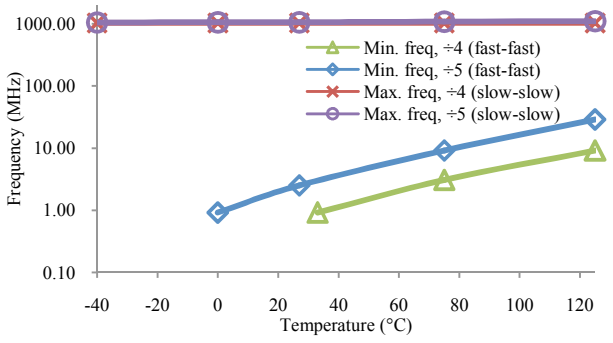

Fig. 9. Simulated frequency range of the divider for worst cases for temperature ranging from -40°C to 125°C. The designed circuit is fully functional as a dual modulus divider with locking range 28.57 MHz - 1.026 GHz across the simulated temperature range.

The MC switch adds extra parasitic capacitance at node A, resulting in exacerbated charge sharing between A and OUT2. This causes a significant rise in the 'low' OUT2 signal when OUT1 becomes 'low' and slightly turning on M_1 (with M_3 not present). During this phase, the footers are also turned 'on' by IN. As a result, charge in OUT3 leaks through M_2 and the footer and OUT3 decays. At low frequency and high temperature, this leakage can be sufficient to cause an erroneously 'low' level at OUT3. To prevent this, a minimum-size NMOS M_3 is added in series with M_2. This causes a negative V_{GS} for M_2, which reduces the leakage. Using two series transistors also avoids the reverse short-channel effect, which would decrease the threshold voltage and increase leakage in a single longer transistor. Also, node A has been laid out to have minimum wiring area to reduce its capacitance.

It is to be noted that adding M_3 limits the high frequency operation in ÷4 mode to a small extent, by slowing the rising and falling edges of OUT2 and OUT3 respectively. If low-frequency operation is not a priority, M_3 may be omitted.

III. Results

A. Locking Range

Post-layout simulations of the proposed divider show its robust performance across a wide frequency and temperature range. The divider's simulated locking range for different temperatures and process corners is shown in Fig. 9. The plot shows results from simulations of the worst-case scenarios. These scenarios are 1) fastest corner at lowest frequency at highest temperature, where leakage will be highest while not disrupting divider's operation, and 2) slowest corner at highest frequency at lowest temperature, where edge-times will start to be large enough to upset divider's operation. These simulations predict the divider's dual-modulus locking range to be about 28.57 MHz to 1.026 GHz, or 189%. The proposed divider achieves this locking range over a temperature range from -40°C to +125°C, which includes the commercial and industrial temperature ranges. The divider reaches its high-frequency limit in ÷4 mode at -40°C, while in ÷5 mode, the limit increases about 50 MHz across the temperature range.

B. Power consumption

Over the locking range of 28.57 MHz – 1.026 GHz, simulated total power consumption, from a 1 V supply, by the divider and the buffers ranges from 243.5 nW to 8.5 µW in ÷4 mode at room temperature. At room temperature and 400 MHz (MICS band), power consumption is 3.35 µW and 3.13 µW in the ÷4 and ÷5 modes, respectively. Most of this power is consumed by the input buffer (about 2.22 µW). The divider's functionality does not depend on input signal's power as the divider needs a digital input signal to its input buffer, which has a minimum sized first stage. Fig. 10 shows power consumption at different frequencies from a 1 V supply at 27°C temperature and typical process corner.

Figure of Merit (FOM), defined by input frequency in GHz divided by power consumption in mW, of this divider is 119.4 GHz/mW in ÷4 mode.

TABLE I
PERFORMANCE COMPARISON WITH EXISTING WORKS

	Topology	Process	Power	Division Ratio	Locking Range (GHz)	% Locking Range	FOM (GHz/mW)
[1]	Dynamic logic	0.35 µm	2.5 mW	2	1 – 5.2	135.5	1.24
[2]	ILFD	90 nm	3 µW	5	0.37 – 0.66	56	134
[3]	ILFD	90 nm	0.8 mW	2	35.7 – 54.9	42	68.8
[4]	ILFD	0.2 µm	44 µW	2	2.0 – 4.3	73	97.7
[5]	ILFD	0.18 µm	12.51 mW @ 1.8 V	3	4.85 – 5.7	16.11	0.4
[6]	ILFD	90 nm	28 µW	2/3	0.379-0.542	35.4	14.3
[8]	LILFD	0.18 µm	3.6mW@1.8 V	8	9.2 – 12.3	30	3.1
This work	Hybrid	90 nm	3.35 µW	4	0.029 – 1.026	189	119.4
			3.13 µW	5	0.009 – 1.098	199.7	127.8

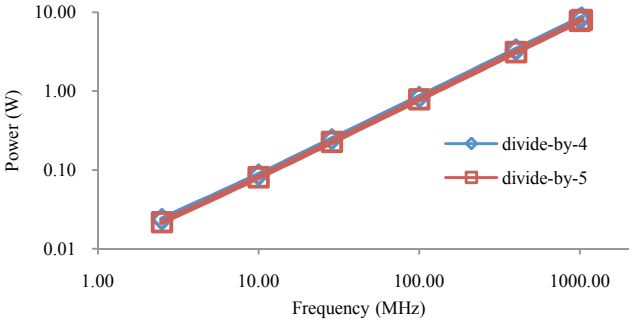

Fig. 10. Power consumption at different frequencies at 1 V supply, 27°C and typical process corner.

C. *Functionality under Low Supply Voltage*

The proposed dual-modulus divider can maintain its functionality at MICS band with a supply voltage as low as 0.8 V. Below this voltage, 'low' half-cycles of injected input become too narrow to accommodate the slow rising edges of OUT signals. At 0.8 V supply, simulation predicts the divider's power consumption to be only 2.62 µW (÷4) or 2.47 µW (÷5). Figure of Merit, in this case, is 152 GHz/mW, which surpasses that of existing works for dividers of this range of frequency.

D. *Comparison with Existing Works*

Simulations predict significantly improved performance of this divider relative to existing works. A comparative overview of this work and some other recently published dividers is given in Table 1. It can be seen that the new hybrid topology consumes lower power than most existing dividers. The ILFD in [2] consumes slightly less power, but operates over a smaller locking range. The proposed divider achieves a much wider locking range than existing ILFDs and, unlike most low-power dividers, also features dual-modulus operation.

IV. CONCLUSIONS

A ring-oscillator-based dual-modulus frequency divider is proposed with post-layout simulation results. A summary of simulated performance is given in Table 2.

TABLE II
PERFORMANCE SUMMARY

Technology	90 nm CMOS process
Silicon Area	45 µm^2
Locking range	28.57 MHz – 1.098 GHz (189%) (÷4)
	9.09 MHz – 1.026 GHz (196%) (÷5)
Operating temperature	-40°C – 125°C
Power consumption @ 400MHz, 1 V, 27°C	3.35 µW (÷4)
	3.13 µW (÷5)

Post-layout simulations across all corners predict this divider to have 189% locking range with high robustness with temperature for both division ratios. This operating range covers MICS band and three ISM bands. The divider only consumes about 3.3 µW at MICS band from 1 V supply at room temperature. Power consumption at MICS band can be minimized by reducing supply to 0.8 V, where only 2.622 µW is required at ÷4 mode.

V. REFERENCES

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