A Sub-Microwatt Low-Noise Amplifier for Neural Recording

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***Abstract*— In this paper we present a pre-amplifier designed for neural recording applications. Extremely low power dissipation is achieved by operating in an open-loop configuration, restricting the circuit to a single current branch, and reusing current to improve noise performance. Our amplifier exhibits 3.5μVrms of input-referred noise and has a digitally-controlled gain between 36dB and 44dB. The amplifier is AC-coupled, with a pass-band from 0.3 Hz to 4.7kHz. The circuit is implemented in a 0.5μm SOI Bi-CMOS process and consumes 805nA from a 1.0V supply, corresponding to a noise efficiency factor (NEF) of 1.8, which is the lowest reported NEF to date.**

I. Introduction

Over the past several years implantable neural interfaces have demonstrated the potential to profoundly improve the quality of life for persons with severe impairments [1]. Power dissipation is a critical constraint for implantable devices because of available power sources, required battery lifetimes, and thermal damage to tissue. Because the signals of interest are so small, the front-end amplifier often consumes a substantial fraction of the overall system power [2] to reduce the noise contribution to acceptable levels. Future neuroprosthetic systems will demand massively parallelized arrays of hundreds of neural recording amplifiers, mandating a strict minimization of amplifier power consumption.

Recently there has been a great deal of research into the design of low-power amplifiers for neural recording[3][4][5]. The large majority of previous work has focused on conventional closed-loop amplifiers built from operational amplifiers. Open-loop amplifiers can give superior noise performance for a given power budget at the expense of linearity performance, imprecise gain control, and reduced power-supply rejection. At the core of our design philosophy are techniques to maximize noise efficiency at the expense of linearity and supply rejection. This tradeoff is warranted due to the unique nature of the of the neural recording problem.

The small signal levels ($\sim$100μV) of neural signals relax linearity requirements relative to those for general purpose amplifiers. If the application is the detection of action potentials, then precise signal reconstruction is not as important as preservation of relative amplitudes, further relaxing both linearity requirements and the need for precisely defined gain. Provision of a stable power supply should be possible with careful system design. Implantation in the human body provides some shielding of the power supply against interferers such as 50Hz/60Hz noise. Low current consumption and low voltage requirements also ease the task of generating a stable supply.

The signal energy of action potentials lies above 100Hz, with estimates for the upper frequency limit ranging from 3.1kHz [6] to 6kHz [7].

II. Design

A schematic of the amplifier is shown in Fig. 1. We used MOS-bipolar pseudo-resistors (PR) [3] to implement the AC coupling necessary to reject large DC offsets due to contact potentials. Each of the transistors in the pseudo-resistor is connected such that there is a MOS diode and a parasitic source-bulk diode connected in anti-parallel. If the voltage across the device is small, then neither diode will conduct strongly, and the effective resistance is very large ($>$10GΩ). The voltage across PR1 is limited to the magnitude of the input signal, while the voltage across PR2 is dictated by the output signal. In order to keep the pseudo-resistor in the high-resistance region, two devices are connected in series.

We have utilized two strategies to minimize the input-referred noise. The first is to limit the number of current branches. The proposed amplifier has only one branch operating at full current. The reference current is ten times smaller than the amplifier bias current, so it does not contribute significantly to the total power consumption. The same RC network used to AC couple the PMOS input presents a low-pass filter to the reference transistor MP0, so noise from the current reference is not added to the signal.

The second strategy is to drive the gates of both MP1 and MN1. A conventional common-source amplifier has a current-source load which adds noise to the signal, but performs no amplification. Because the input must be AC-coupled, it is possible to decouple the DC levels of the gates of transistors MP1 and MN1 while keeping them connected in the frequency band of interest. The amplifier's transconductance is effectively doubled, while output noise remains constant, reducing the input-referred noise voltage by a factor of two.

The aspect ratios of MP1 and MN1 were chosen to place both transistors in the weak inversion regime in order to maximize g_m/I_D. The lengths of the transistors MP1 and MN1 were chosen to be large to obtain sufficient gain from a single stage and to yield an acceptable level of $1/f$ noise, which is inversely proportional to gate area [8]. The bias current is generated from an on-chip bias circuit based on [9] and multiplied by a 3-bit digitally-controlled current mirror. The bias current in the amplifier can be varied from 110nA to 770nA.

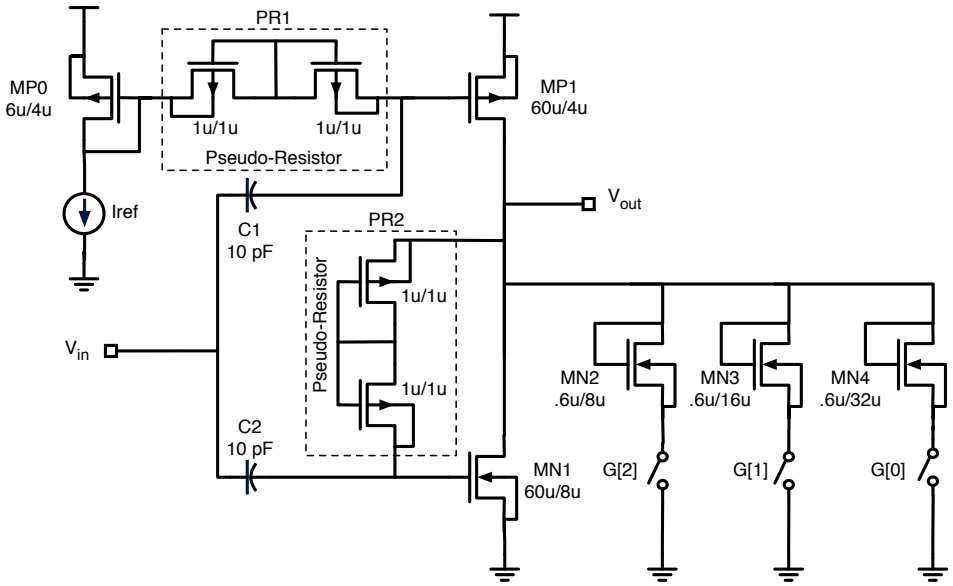

Fig. 1. Schematic of the amplifier.

Our amplifier includes a bank of digitally-enabled diodes M2-M4, which allow the user to control the gain through the gain-control word G[0:2]. The aspect ratio of MN2 is 100 times smaller than that of MN1, and $V_{GS,1}$=$V_{GS,2}$, so the incremental conductance of MN2 is approximately 100 times smaller than $g_{m,MN1}$. In the absence of any channel-length modulation, and assuming equal subthreshold slope factors (and thus equal g_m) for MN1 and MP1, MN2 would limit the gain to 200. This scheme was used to provide a relatively well-controlled gain in an open-loop amplifier. Including the effect of channel-length modulation, MN2 reduces the gain by about 6 dB, from 44.3dB to 38.4dB. With M3 and M4 enabled, the gain drops to 36.1dB.

III. Results

We fabricated our amplifier in a .5µm SOI-BiCMOS process and employed CMOS devices exclusively. The amplifier occupies .033 mm^2 and the current reference occupies .013 mm^2 of die area. The circuit can operate from a supply between 1V and 5V. The measurements presented here were taken with a 1.0V supply.

Fig. 3 shows the frequency response over the entire range of gain settings. The current reference is configured to provide the maximum bias current, yielding $I_{DS} = 770\text{nA}$ for MP1 and MN1. At the highest gain setting, the amplifier exhibits a gain of 44dB and bandwidth of 1.9kHz. The intermediate gain setting provides a gain of 38dB of gain and a 3-dB frequency of 3.6kHz. With the lowest gain setting, the gain is 36dB, and the 3-dB frequency is extended to 4.7kHz. For the remainder of this section we will focus primarily on the low-gain setting, because it provides sufficient bandwidth to record action potentials.

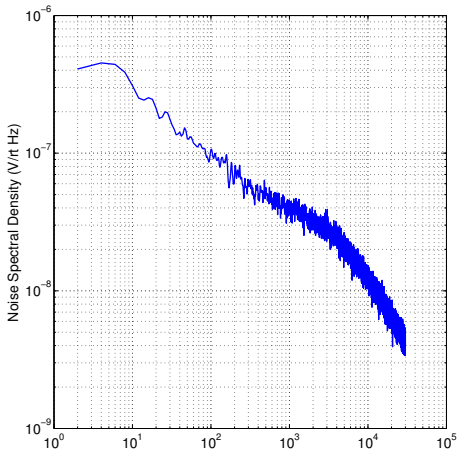

Fig. 2. Input-referred noise spectrum of the amplifier, computed as the measured output noise spectrum divided by the mid-band gain.

The input-referred noise spectrum of the amplifier is shown in Fig. 2. Despite the large transistor sizes, $1/f$ noise dominates. The total RMS noise at the input is 3.5µV. It is difficult to discern the white thermal noise region of the spectrum because of the proximity of the $1/f$ noise corner to the output pole of the amplifier, but analysis predicts an input-referred thermal noise density of about $20\text{nV}/\sqrt{\text{Hz}}$.

Feedback amplifiers achieve high linearity because their gain is determined by ratioed passive components. For open-loop amplifiers, nonlinearity of the transconductance and of the output impedance is manifested in a nonlinear input-output function. The linearity of the proposed amplifier can

TABLE I

COMPARISON OF NEURAL AMPLIFIERS

	Gain	I_{Amp}	NEF	$v_{ni,RMS}$	THD (@ Input)	PSRR	$Bandwidth$	Area	Tech.
This work	36.1dB	805nA	1.8	3.6μV	7.1% @ 1mVpp	5.5dB	.3Hz-4.7kHz	.046mm^2	.5μm
Harrison [3]	39.5dB	16μA	4.0	2.2μV	1% @ 16.7mVpp	$\geq$ 85dB	.025Hz-7.2kHz	.16mm^2	1.5μm
Denison [4]	45.5dB	1.2μA	4.9	.93μV	—	—	.5Hz-250Hz	—	0.8μm
Wu [5]	40.2dB	330nA	3.8	.94μV	.053% @ 5mVpp	62dB	3mHz-245Hz	—	.35μm

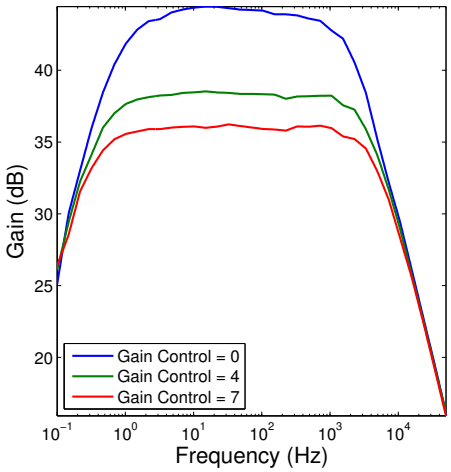

Fig. 3. The frequency response of the amplifier with three different gain settings. The gain adjustment number refers to the digital gain control word G[0:2] in Fig. 1.

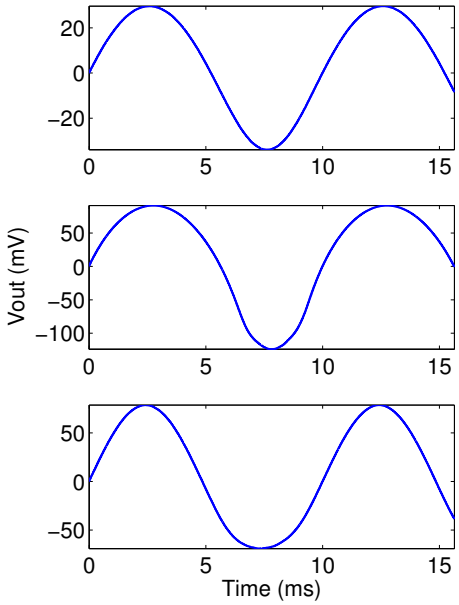

Fig. 4. Output voltage waveforms for 100Hz sinusoidal input. (Top) Low gain setting, peak-to-peak amplitude of 1mV. (Middle) Low gain setting peak-to-peak amplitude of 10mV. (Bottom) High gain setting, peak-to-peak amplitude of 1mV.

be assessed visually in Fig. 4, which shows output waveforms corresponding to a 100Hz input with various amplitudes. In the top waveform, with peak-to-peak input amplitude of 1mV, the distortion is not visually noticeable. With a 10mV input, the incremental resistance of the gain-control transistors MN2-4 decreases at the upper end of the range, causing substantial compression. For the third waveform, the amplifier is in the high-gain configuration, and the input amplitude is 1mVpp. Fig. 5 shows the power spectra of the same three waveforms shown in Fig. 4. THD with the 10mV input is quite high at 18.12%, but for a 1mVpp input, THD is lower, at 7.06% and 6.63% for the low and high gain settings, respectively.

In applications where a quiet power supply cannot be guaranteed, power-supply rejection ratio must be examined. In the proposed amplifier, both MP1 and MN1 have their sources connected to a power supply and their gates capacitively connected to the input. Thus, the positive and negative supplies directly modulate the P- and N-type transconductors, respectively. Therefore we expect that the gain from the power supply to the output will be approximately half the gain from input to output, resulting in a minimal PSRR of 6dB. Fig. 6 shows the positive power-supply rejection ratio from 20Hz to 20kHz, which is an average of 5.5dB between 1Hz and 100Hz, and improves between 100Hz and 30kHz. Because of the weak supply rejection, the output will be susceptible to supply noise existing in the frequency band of interest.

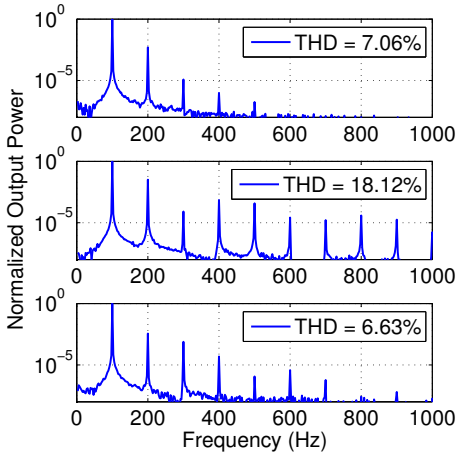

Fig. 5. The output power spectrum with the amplifier input driven by a 100Hz sinusoid. At the top the amplifier is configured for low gain (G=7) with a 1mVpp input. The middle plot also shows the low gain configuration with a 10mVpp input. The bottom plot shows the high gain configuration (G=0) with a 1mVpp input.

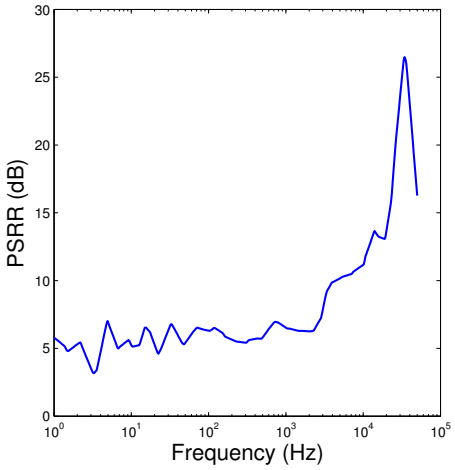

Fig. 6. Power-supply rejection ratio.

In Table I we compare the performance of our amplifiers to other recently published biosignal amplifiers. To compare our noise and power performance to other amplifiers, we use the noise efficiency factor (NEF), introduced in [10]:

$$\text{NEF} = V_{rms,in}\sqrt{\frac{2 \cdot I_{Total}}{\pi \cdot U_T \cdot 4kT \cdot BW}} \qquad (1)$$

where I_{Total} is the total amplifier current, U_T is the thermal voltage, BW is the amplifier bandwidth, $V_{rms,in}$ is the input referred RMS noise voltage. For consistency with other work, the current specified in Table I excludes the current consumed by the bias generator, which consumes an additional 27nA. Our amplifier demonstrates the lowest NEF of any amplifier reported to date. Including the bias circuitry, the entire amplifier chip dissipates less than 1μW.

IV. Conclusions

We have presented a novel amplifier which allows excellent power efficiency to be obtained at the expense of linearity, supply rejection, and gain accuracy. Our amplifier exhibits the lowest NEF published to date. The low power and area provided by this design would allow the realization of a 256-channel amplifier array with an area of 8.4mm^2 and a power dissipation of 206μW. For power-limited implantable neural recording applications focused on detection of action potentials, our amplifier demonstrates an attractive tradeoff of power and performance.

V. Acknowledgements

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