

ECE 551 Design Vision Tutorial

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Lesson 0	– Tutorial Setup.....	2
Lesson 1	– Code Input (Analyze and Elaborate).....	4
Lesson 2	- Simple Synthesis.....	8
Lesson 3	– Design Constraints	10
Lesson 4	– Reports	19
Appendix A	– Synopsys Code Directives.....	30
Appendix B	– Extra Optimization	32
Appendix C	- Reports Output	35
1.	Report Design	35
2.	Report Design Hierarchy	36
3.	Report Reference	40
4.	Report Wire Loads.....	41
5.	Report Ports	42
6.	Report Cell.....	53
7.	Report Net.....	55
8.	Report Clock	62
9.	Report Area.....	62
10.	Report Compile Options	63
11.	Report Power	64

Lesson 0 – Tutorial Setup

For this tutorial you must not use the GNOME User Interface. The program will not open in that environment. You may use any of the other available window environments.

1. In your root directory, go to your ece551 directory (as should have been created in the modelsim tutorial)

```
%> cd ece551
```

2. Copy all files from ~ece551/public_html/tutorials/designvision to your current directory

```
%> cp -r ~hickmann/public_html/tutorials/designvision .
```

3. Change directory to your tutorial directory

```
%> cd designvision
```

4. Copy file from current directory to root directory

```
%> cp .synopsys_dc.setup ~/
```

5. Change to the main tutorial directory

```
%> cd dv_tutorial/risc_design
```

It is important to start Design Vision from the directory where your project is so that environment variables that are automatically setup will be made correctly.

IMPORTANT

If you see that the design variables do not match later on in the tutorial do the following:

*In the directory you started Design Vision in remove the .synopsys_dc.setup file.

```
%> rm .synopsys_dc.setup
```

This will force design vision to use the one from your root directory.

6. Start Design Vision. Make sure to use the newver command to run the latest version on the Linux machines. The older version will only run on the Sun machines.

```
%> newver design_vision
```

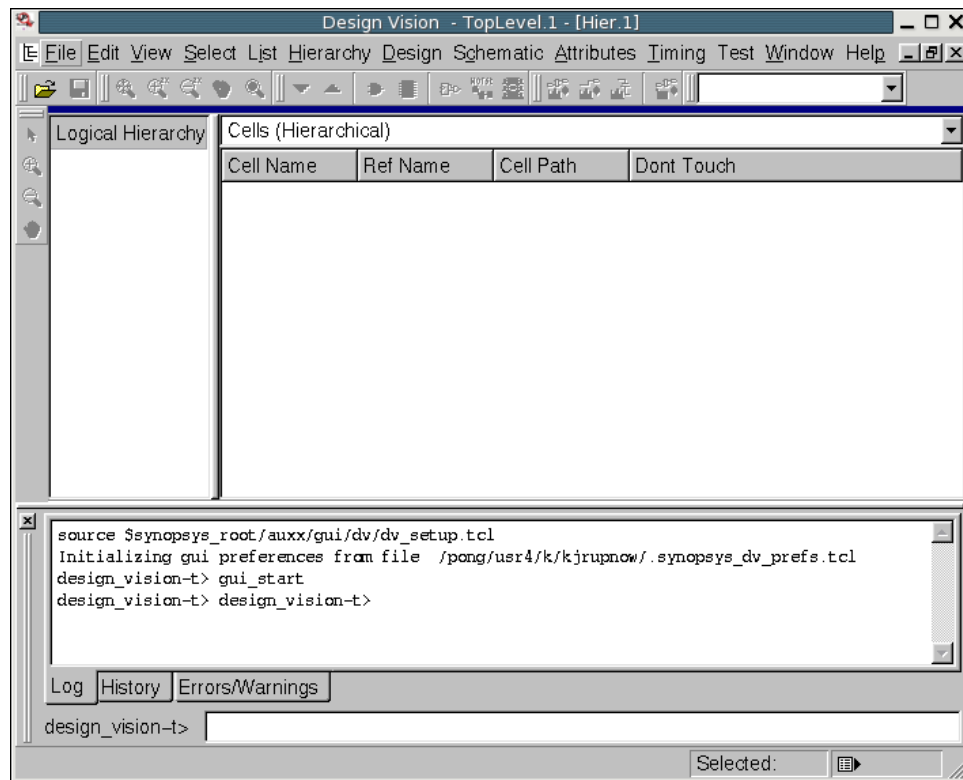


Figure 0-1 : Design Vision Default Window

We may look at the main window of Design Vision to see a few of the program's features. In the top panel, there are two panes. The left pane is a full Hierarchy pane; it will show the entire hierarchy of the current design (as selected from the drop-down box in the upper control panel). The right pane is a context based panel which will display contents based upon the selection in the drop down box at the top of the panel.

The bottom panel has three different tabs: log, history and errors/warnings. The important thing to note about this panel is that every command you perform will appear in this panel, allowing you to learn the commands and create scripts of commands for future use. It is also the panel that you must monitor to determine the source of errors and warnings, allowing you to fix the code or correctly determine if a warning is expected.

Lesson 1 – Code Input (Analyze and Elaborate)

1. Analyze RISCTYPES.VHD first
File->Analyze

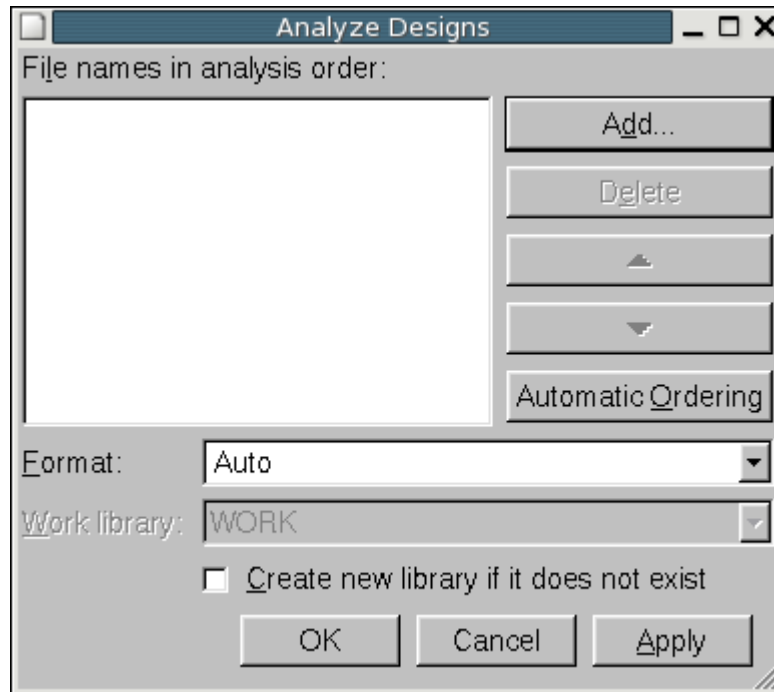


Figure 1-1 : Analyze Design Dialog

Click Add
select source/RISCTYPES.VHD

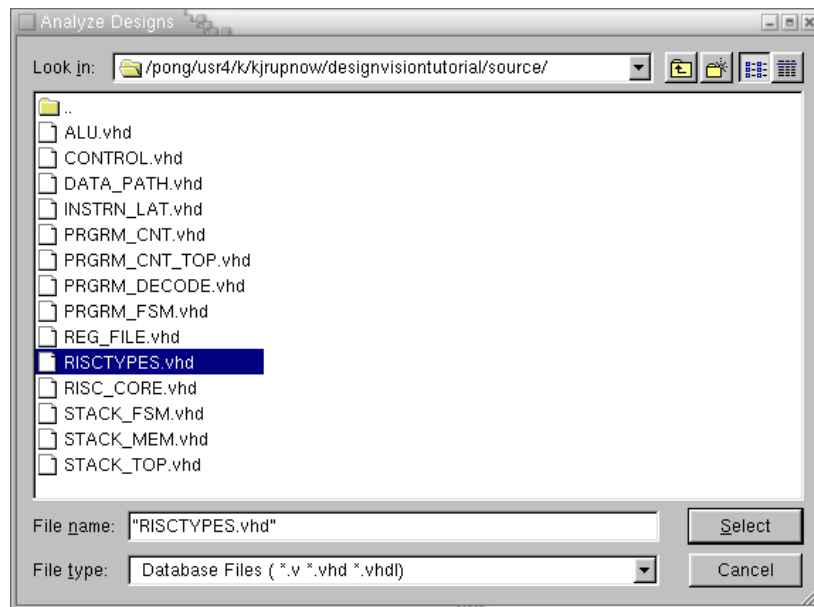


Figure 1-2 : Analyze Design Dialog

Click OK

2. Now analyze the rest of the files

File->Analyze

Click Add...

Select All Files in /source Except RISCTYPES.VHD

Note that the reason we must analyze in a specific order is because of some of the ordering requirements of VHDL, so no particular order will be required when using Verilog code with Design Vision

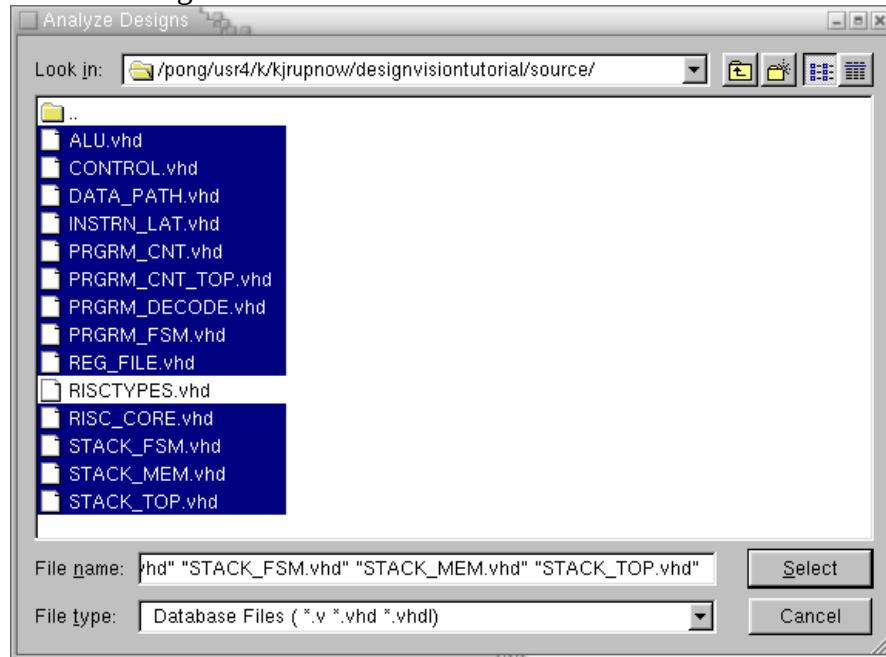


Figure 1-3 : Analyze Design Dialog (2)

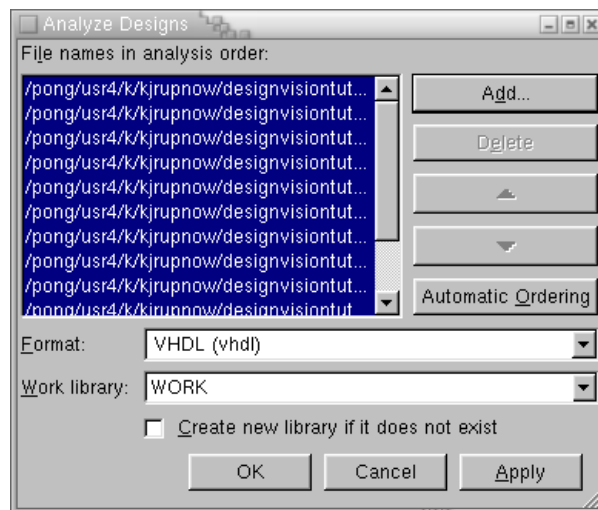


Figure 1-4 : Analyze Designs Dialog

Analyze is similar to compilation. It will check the syntax of each of the files to verify correct use of the language and that all code used is synthesizable.

```

Initializing gui preferences from file /pong/usr4/k/kjrupnow/.synopsys_dw_prefs.tcl
design_vision-t> gui_start
design_vision-t> analyze -library WORK -format vhd1 {{/pong/usr4/k/kjrupnow/designvisiontutorial/source/RISCTYPES.vhd}}
Loading db file '/usr/apps/eda/synopsys/syn_U-2003.06/libraries/syn/standard.sldb'
Loading db file '/usr/apps/eda/synopsys/syn_U-2003.06/libraries/syn/dw_foundation.sldb'
Loading db file '/usr/apps/eda/synopsys/syn_U-2003.06/libraries/syn/gtech.db'
Loading db file '/usr/apps/eda/flexstream.3.3/lsi_fs_3.3/lib3p/synopsys/gflxp/gflxp_lsi_wc.db'
Loading db file '/usr/apps/eda/flexstream.3.3/lsi_fs_3.3/lib3p/synopsys/gflxio/gflxio_lsi_wc.db'
Reading in the Synopsys vhd1 primitives.
/pong/usr4/k/kjrupnow/designvisiontutorial/source/RISCTYPES.vhd:
design_vision-t> analyze -library WORK -format vhd1 {{/pong/usr4/k/kjrupnow/designvisiontutorial/source/STACK_TOP.vhd}} {{/pong/usr4/k/kjrupnow/designv
/pong/usr4/k/kjrupnow/designvisiontutorial/source/STACK_TOP.vhd:
/pong/usr4/k/kjrupnow/designvisiontutorial/source/STACK_MEM.vhd:
/pong/usr4/k/kjrupnow/designvisiontutorial/source/STACK_FSM.vhd:
/pong/usr4/k/kjrupnow/designvisiontutorial/source/RISC_CORE.vhd:
/pong/usr4/k/kjrupnow/designvisiontutorial/source/REG_FILE.vhd:
/pong/usr4/k/kjrupnow/designvisiontutorial/source/PRGRM_FSM.vhd:
/pong/usr4/k/kjrupnow/designvisiontutorial/source/PRGRM_DECODE.vhd:
/pong/usr4/k/kjrupnow/designvisiontutorial/source/PRGRM_CNT_TOP.vhd:
/pong/usr4/k/kjrupnow/designvisiontutorial/source/PRGRM_CNT.vhd:
/pong/usr4/k/kjrupnow/designvisiontutorial/source/INSTRN_LAT.vhd:
/pong/usr4/k/kjrupnow/designvisiontutorial/source/DATA_PATH.vhd:
/pong/usr4/k/kjrupnow/designvisiontutorial/source/CONTROL.vhd:
/pong/usr4/k/kjrupnow/designvisiontutorial/source/ALU.vhd:

```

Figure 1-5 : Analyze Results Log

3. Elaborate the design

File->Elaborate
Change Library to WORK
Change Design to RISC_CORE(struct)
Click OK

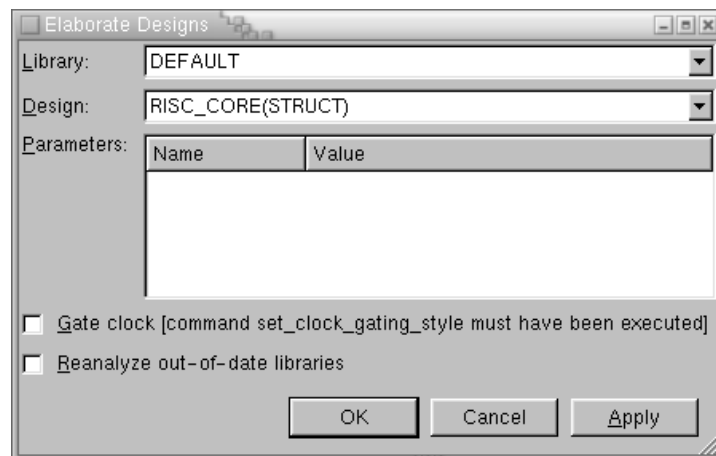


Figure 1-6 : Elaborate Dialog

The elaboration step may take several minutes. This step is similar to loading the design in Modelsim. The design is checked to make sure that the code is synthesizable, the sub-designs connect correctly and that there are no major errors in the implied circuit. (At the end of this step you may determine that latches were incorrectly implied and fix your code to remove them).

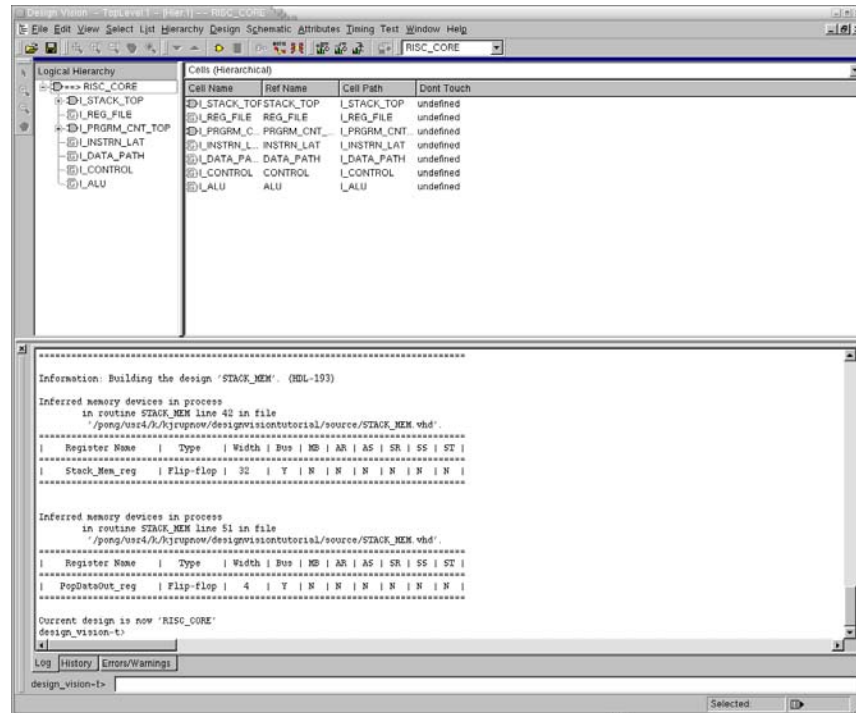


Figure 1-7 : Main Window After Elaboration Step

Now that we have elaborated the design, we see some basic structure of the design in the main window of Design Vision. The left pane of the main window shows the full hierarchy of the design starting from the design that is specified as the top-level (from the drop-down box in the top tool panel). In the right pane we can select what we see to help perform later tasks. By right clicking on a module, we may also choose to see a schematic view from the right click menu. The schematic view may be useful, but requires a good understanding of synthesis, as the module names may seem cryptic at first.

Lesson 2 - Simple Synthesis

Now that we have analyzed and elaborated the design, we can perform simple synthesis on our design. In ECE 551, we will require the use of design constraints which will be covered in Lesson 3, however we may see some information about the design by performing an unconstrained compilation.

In mapping options we may specify mapping and area effort. Map effort refers to how long the synthesizer will work towards a better organization of the cells before moving on to the next stage. Area effort refers to how long the synthesizer will try to reduce the area of the design before moving on to the next stage. Power effort indicates how long the synthesizer will try to optimize the power used by your circuit. Other compile options are:

1. Top Level – compiles only the top level of the design, leaving the rest uncompiled
2. Ungroup All – Ungroups the entire hierarchy so that all logic is compiled as one module
3. Scan – Refers to the insertion of scan chains for testing logic. This should not be used for this course.
4. Incremental mapping – specifies that the mapping should be done based upon only local information instead of global information. Furthermore, if some mapping information is already available, the synthesis will start from the previous map. This is especially useful when trying to improve upon an initial synthesis
5. Allow boundary conditions – allows that boundary conditions such as known input constants can be used to help optimize the design
6. Auto Ungroup – when enabled, you may choose either area or delay as the trigger, and the synthesizer will automatically ungroup designs to meet constraints if the constraints are not being met for the trigger

Design->Compile Design
Leave options as is and click OK

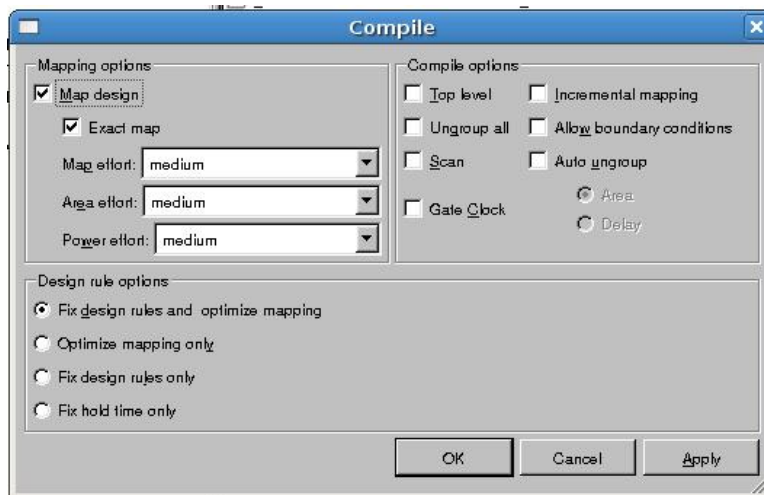


Figure 2-1 : Compile Design Dialog

Compile Ultra uses the same options, which have the same meaning as previously described. The difference is that all effort options are automatically set at their highest levels and the synthesizer automatically picks options to achieve the best results. Compile Ultra should be used carefully as it will always take longer time than manually selecting the options.

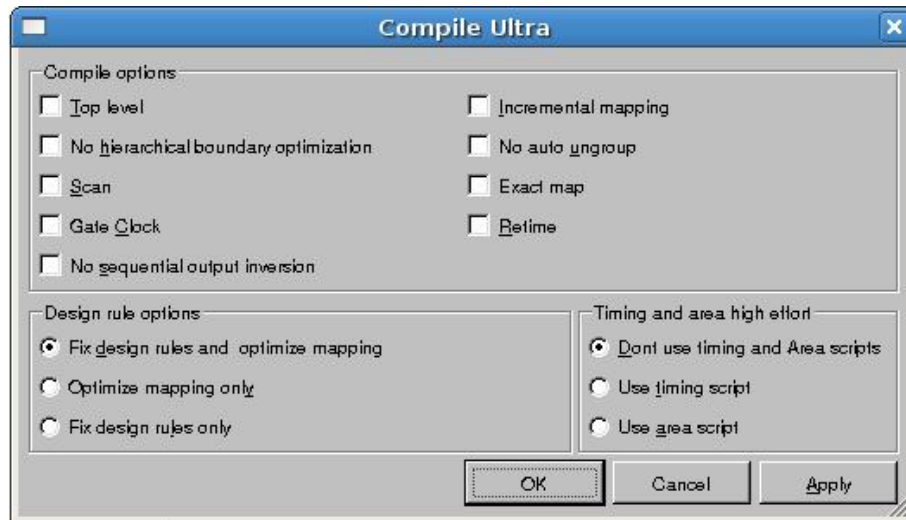


Figure 2-2 : Compile Ultra Dialog

Lesson 3 – Design Constraints

1. Check Design

Performing a design check can find inconsistencies in your design that may or may not be problems. Example check results are having the same input connected to two input ports, and having ports left unconnected (or certain wires within the port left unused).

Design->Check Design

Change Warning messages to "Display in detail"

Change Hierarchy to "Current level and all sub-designs"

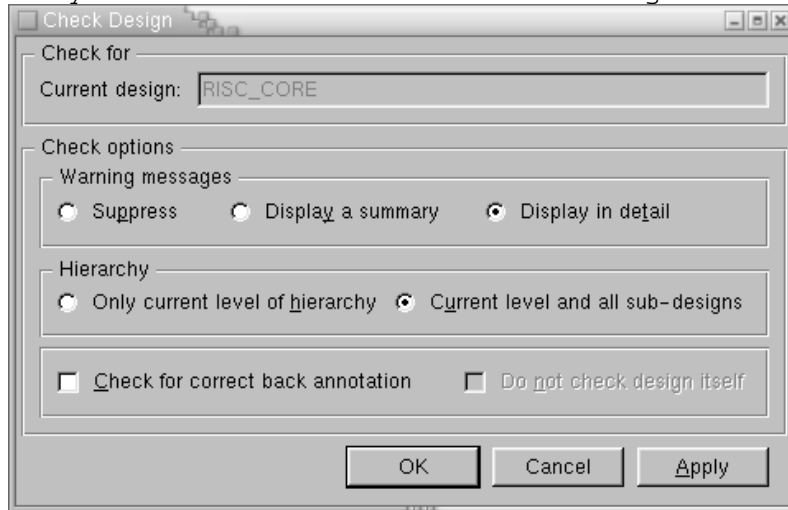


Figure 3-1 : Check Design Dialog Box

The following are some of the warnings that given by the check design command. Note that what is given are warnings. This means that you should check the warnings to ensure they are expected and ok, or change code and/or Design Vision settings before moving on.

Warning: In design 'RISC_CORE', a pin on submodule 'I_STACK_TOP' is connected to logic 1 or logic 0. (LINT-32)

Pin 'PushDataIn[11]' is connected to logic 0.

Warning: In design 'CONTROL', port 'Crnt_Instrn[29]' is not connected to any nets. (LINT-28)

At this point, the module "STACK_MEM" is instantiated 3 times. In design vision, we need each instantiation to be unique so that each instance can be optimized and mapped separately. To do this, we use the function "Uniquify"

Select RISC CORE in the logical hierarchy in the left pane
Hierarchy->Uniquify->Hierarchy

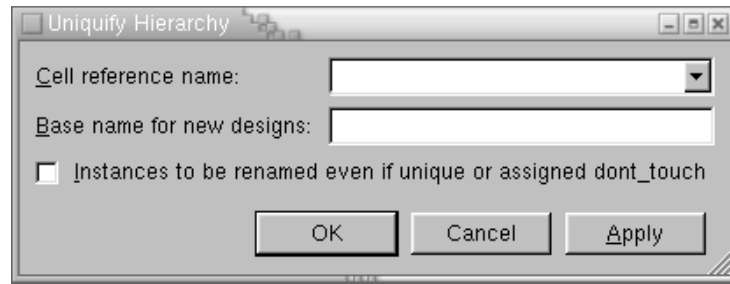


Figure 3-2: Uniquify Hierarchy Dialog

Click OK

This is also done automatically during compilation.

2. Specify Clock

Specify clock tells design vision the clock rate at which the design should be able to operate. This goal will tell design vision to make sure to organize the modules such that calculations can all be performed within the clock period. Various techniques such as logic duplication are used to achieve the goals. It is important to set realistic goals for the clock rate so that design vision does not perform too much logic duplication to attempt to reach the goal.

Choose Ports/Pins in the Hierarchy Window Drop down box
 Select RISC_CORE in the logical hierarchy in the left pane
 Find Clk and select it
 Attributes->Specify Clock

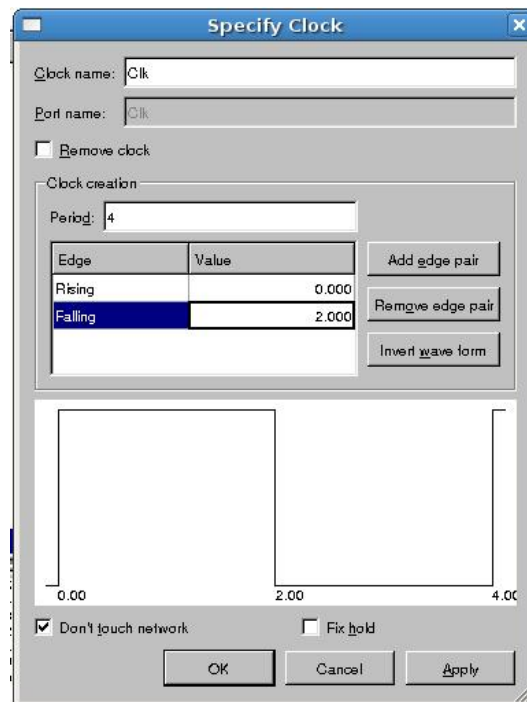


Figure 3-3 : Specify Clock Dialog Box

You will know if you have correctly selected Clk based upon if Clk shows up in the grayed out Port name box. If that box is empty, be sure to close this dialog and make sure Clk is selected before opening this dialog. Since a clock is a signal we don't want to optimize (prevents errors of the synthesizer disconnecting the signal), we want to set the clock as a "don't touch" network. Select Don't touch network before clicking OK.

3. Set Input delay

Input delay tells design vision that a signal will always arrive at a certain time relative to the clock. When specifying delay, the delay should always be specified relative to a clock so that design vision may calculate delays correctly. Change the drop down box to Pins/Ports.

Select->Ports/Pins->Input Ports
Find Clk and Ctrl->Click to unselect it
(we want all input ports except Clk selected)
Attributes->Operating Environment->Input Delay

If you did not select any signals, either the Input Delay option in the menu would be grayed out, or there would be no entries in the Name field.

Select Clk in the Relative to clock dropdown
Specify 2 as the Minimum and Maximum delay

This means that input signals should be modeled so that they arrive 2nS after the edge of clk.

Click OK

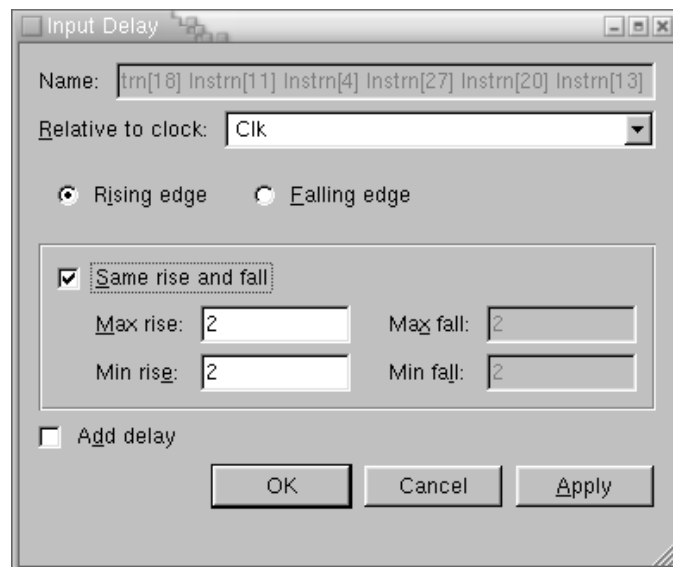


Figure 3-4 : Input Delay

4. Output Delay

Similar to input delay, we must also specify how long an output signal takes to reach the chip's output with respect to the clock. This specifies how long a signal takes to reach the chip's output after leaving your module's output.

Select->Ports/Pins-> Output Ports
Attributes->Operating Environment->Output Delay
Specify 0.5 as the Minimum and Maximum Delay
Click OK

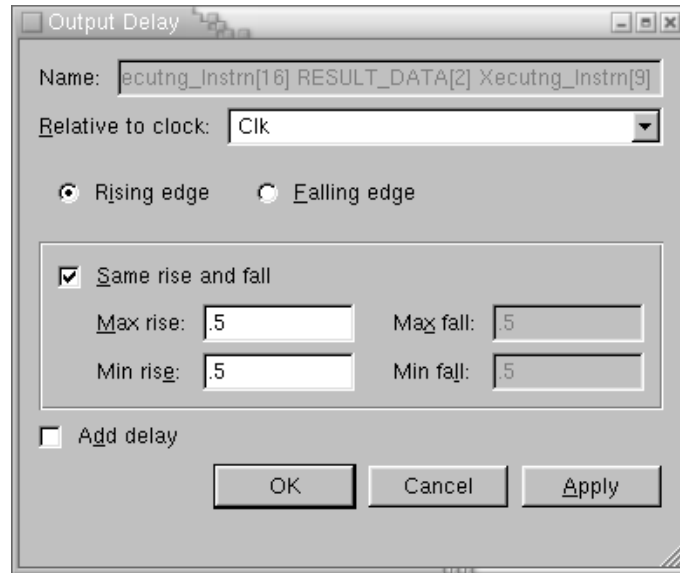


Figure 3-5 : Output Delay

5. Wire Load

We must specify a wire load model so that design vision can estimate the delay that wires in the design have. Each model is based upon a different amount of resistance and capacitance for a certain amount of wire. Design vision will use that amount to estimate how much delay is added to the circuit based on the length of the wires and distance between the wires.

Attributes->Operating Environment->Wire Load
Select B1X1 and Click OK

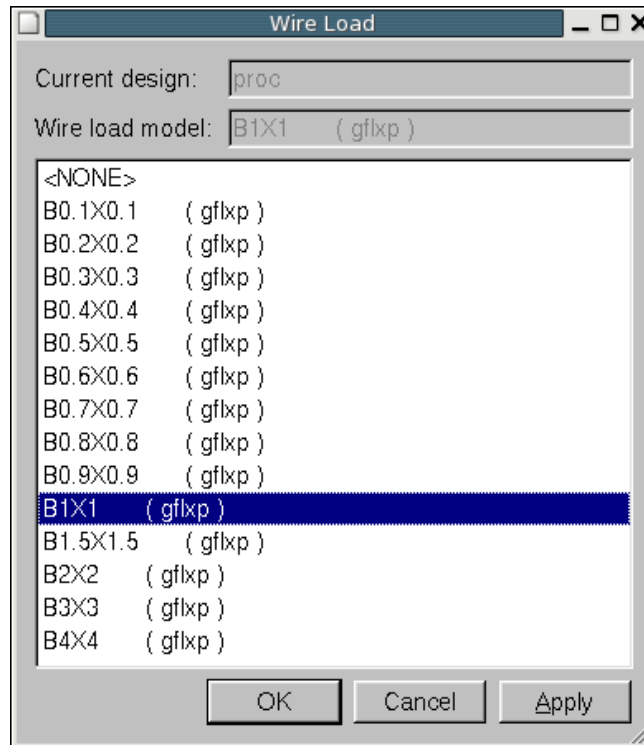


Figure 3-6 : Wire Load Model

6. Operating Conditions

We may specify either single analysis or min/max analysis. Our choice for this option depends upon whether our synthesis library contains one set of analysis information or it contains a set of information for both minimum and maximum cases.

Attributes->Operating Environment->Operating Conditions
Select gflxp as the library and NOM as the Condition, Click OK



Figure 3-7 : Operating Conditions

7. Driving cell

We must specify which cells drive the circuit, and with what strength.

Select->Ports/Pins->Input Pins
Find and Ctrl->Click Clk to deselect it
Attributes->Operating Environment->Drive Strength
Click "Use library cell options"



Click the button

Expand gflxio, find DDRVLS33 and select it

Click the Click to Choose Objects and Click OK

Click OK

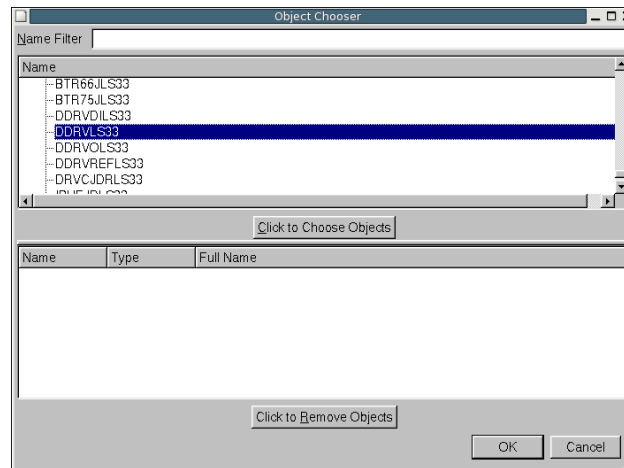


Figure 3-8

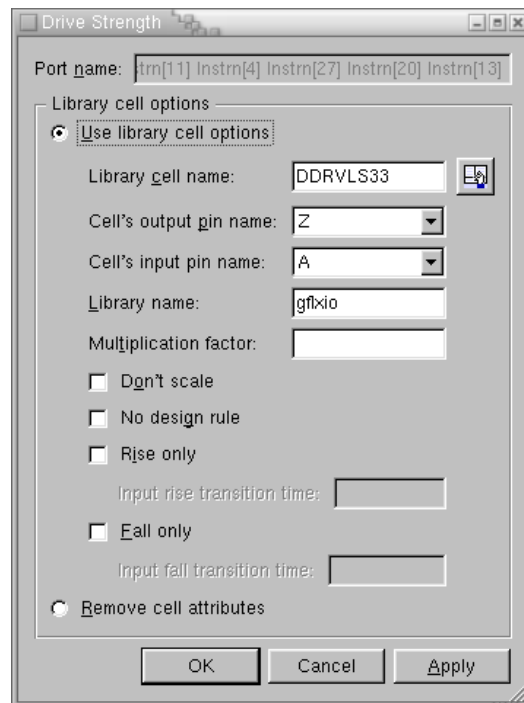


Figure 3-9

8. Top level Constraints

This level of constraints allows us to set overall objectives of the design for design vision to attempt to reach. We can set maximum values for area, power, fanout, and transition. Normally for this course we will only set values for area and fanout, allowing power and transition to vary as design vision likes. This will speed our synthesis time and will allow us to concentrate on the operation of the circuit rather than worrying about power and other effects that require attention after full correctness is guaranteed.

Attributes->Optimization Constraints->Design Constraints
Enter 380000 in the Max Area, click OK

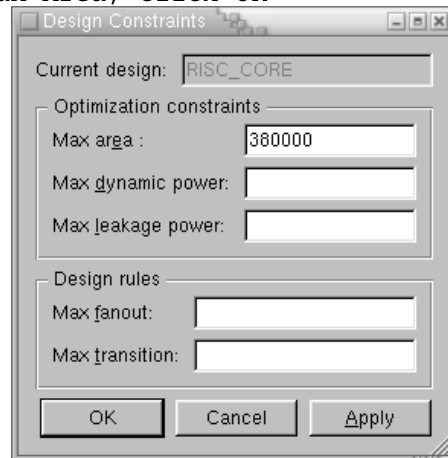


Figure 3-10 : Design Constraints Dialog

9. Output Port Attributes

This option allows us to specify that an output is to be left unconnected or change the signal type. The other signal types available are primarily for use with JTAG (Joint Test Action Group) which allows insertion of testing abilities. We will not need to modify the signal type in this course.

This dialog can be found by doing the following:

Select->Ports/Pins->Output Ports
Attributes->Optimization Directives->Output Port...

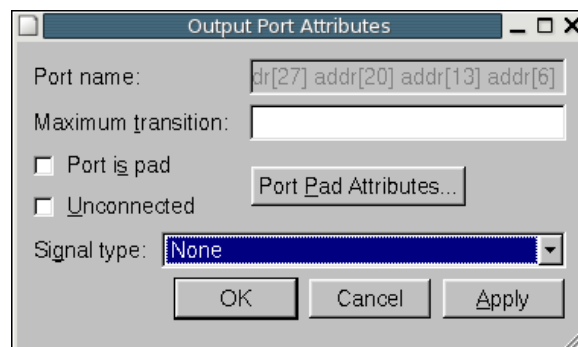


Figure 3-11 : Output Port Attributes Dialog

10. Input Port Attributes

This option allows us to specify different conditions on each input port. We do not need to modify these properties for this course

- a. Maximum fanout – The maximum number of wires that this input can drive before requiring buffers. For example if the max is 10 and we need to connect 100, we connect each of the 10 to a buffer and each of the buffers are connected to 10 of the overall 100.
- b. Maximum transition – The maximum amount of time for the signal to transition from a value to the next value. This allows Design Vision to choose drive strength appropriately to meet the requirement.
- c. Maximum capacitance This setting is not used for ECE 551
- d. Port is pad – Sets the port of the design as a chip level input. This setting is not used for ECE 551
- e. Disable timing This setting is not used for ECE 551
- f. Don't touch network – Tells Synopsys to not modify the network that is specified by the port. Commonly used for Clock and Reset networks which are typically given resources separately from the synthesis process.
- g. Connected to – Allows you to specify that a port is connected to 0, 1 or is exactly the same or exactly opposite of another port. This helps the synthesis process by allowing Design Vision to simplify logic that is connected to these ports.
- h. Test hold – For use with on chip testing features, not used for ECE 551.
- i. Signal type – For use with on chip testing features, not used for ECE 551

This dialog can be found by doing the following:

Select->Ports/Pins->Input Ports
Attributes->Optimization Directives->Input Port...

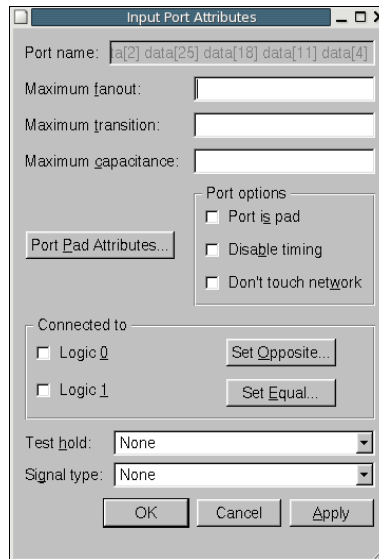


Figure 3-12 : Input Port Attributes

11. Port Pad Attributes

This option allows us to specify how the output (or input) pin on the actual chip will be used. This specification allows design vision to insert (or remove) appropriate logic so that our design operates as expected when placed on chip. This option is not needed for ECE 551 and should not be used.

We have now specified all of the constraints on our design. Before moving on to Lesson 4, you should resynthesize so that the reports you generate will have realistic and interesting data. You may want to revisit Lesson 2 to review the synthesis process.

Additional Constraints that may be used to aid in specifying what kind of optimizations to be performed are found in Appendix B.

When we are using the same constraints repeatedly, we can save the constraints into a script file and simply execute the script. The commands for the file can be taken directly from the commands that are echoed to the log when we executed from the GUI before. To execute a script:

File->Execute Script

Lesson 4 – Reports

We have now finished the entire synthesis process, but need to analyze the results of the synthesis to determine if we need to change code to achieve our goals, or verify that goals have been met. These reports can also be used to offer comparisons of several synthesis attempts. See Appendix C for example results of each of these reports

1. Report Design – This report specifies top level design constraints, such as the library that was used for synthesis, wire load, and operating conditions.

Design->Report Design

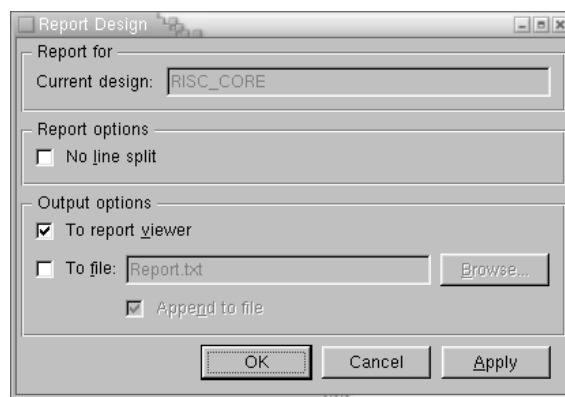


Figure 4-1

2. Report Design Hierarchy – This report will give the entire hierarchy of the design, listing each instance that is used at each level of the hierarchy. In this case we have selected the list first instance option so that in portions of our hierarchy where the same module may be used many times it will be listed only once.

Design->Report Design Hierarchy

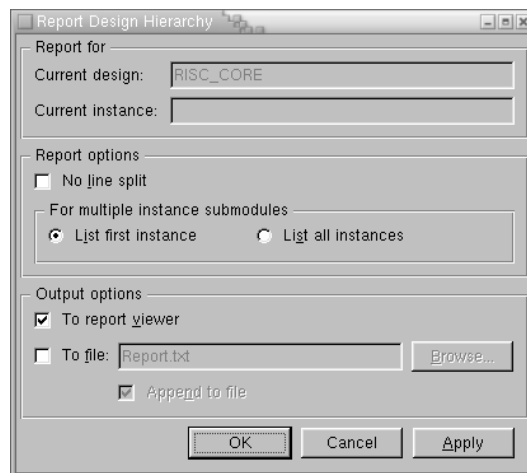


Figure 4-2

3. Report Reference – This report lists all of the references (modules) instantiated on the top level of the design and their corresponding area. This report allows the user to see which modules of their top-level design contribute the most to the overall area of the design.

Design->Report Reference

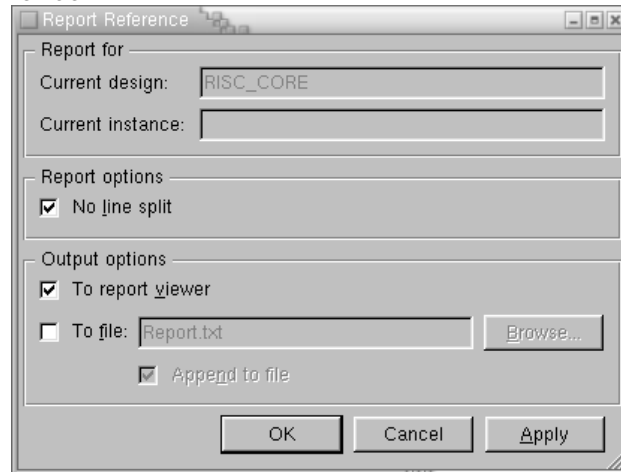


Figure 4-3

4. Report Wire Load – This report lists the wire loads in the design (listing both the wire load model used and some information on the relative occurrence of different amounts of fanout). Note that this report is included in the Report Design report.

Timing->Report Wire Load

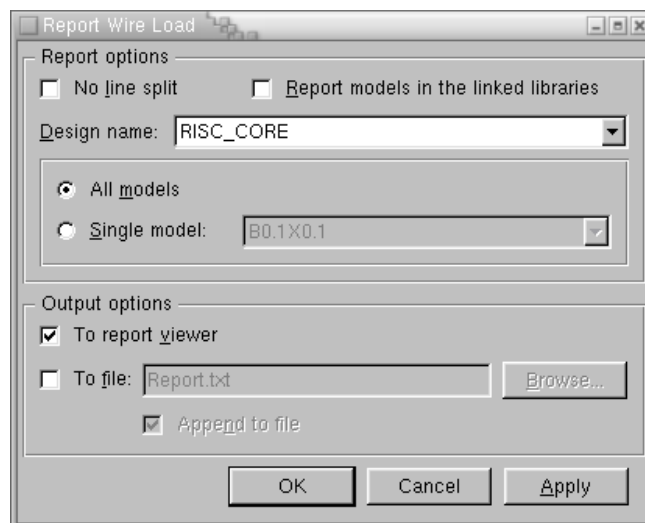


Figure 4-4

5. Report Ports – This report is generated based upon the ports that you currently have selected, or you may manually type the names of the ports or use the 

button to search for the ports you wish to be included in the report. The report will include capacitive load, input or output delay that has been specified, transition time and resistance. Not all of these items may have been calculated or specified depending upon the library you used, so the report will give whatever is available.

Design->Report Ports

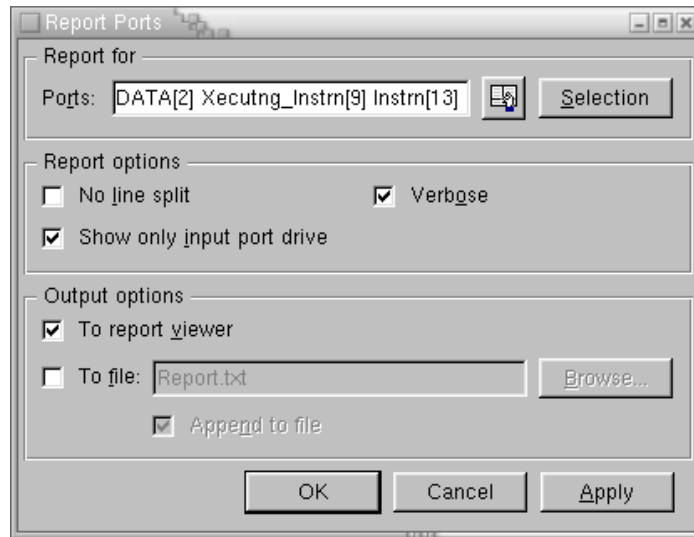


Figure 4-5

6. Report Cells – This report specifies each cell and also shows the connections between cells. For example, the report can show what pins are outputs of a cell, and what library cell type is connected to that output (to see whether the outputs are registered).

Design->Report Cells

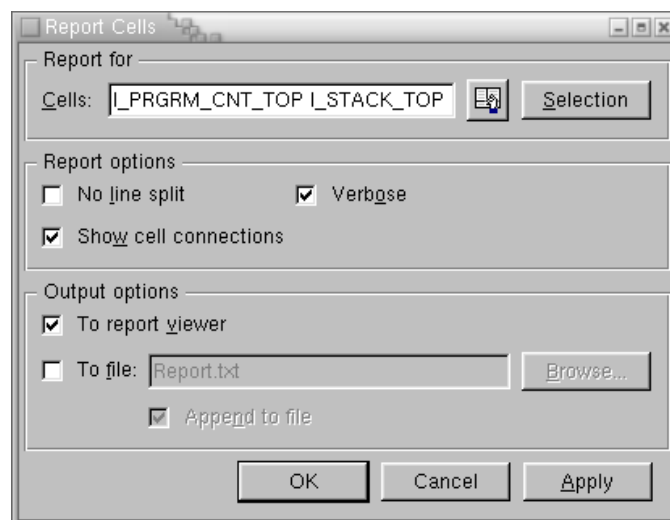


Figure 4-6

7. Report Nets – This report shows direct connections of nets, including transition times, capacitance, resistance, number of input drivers, and number of outputs (fanout).

Design->Report Nets

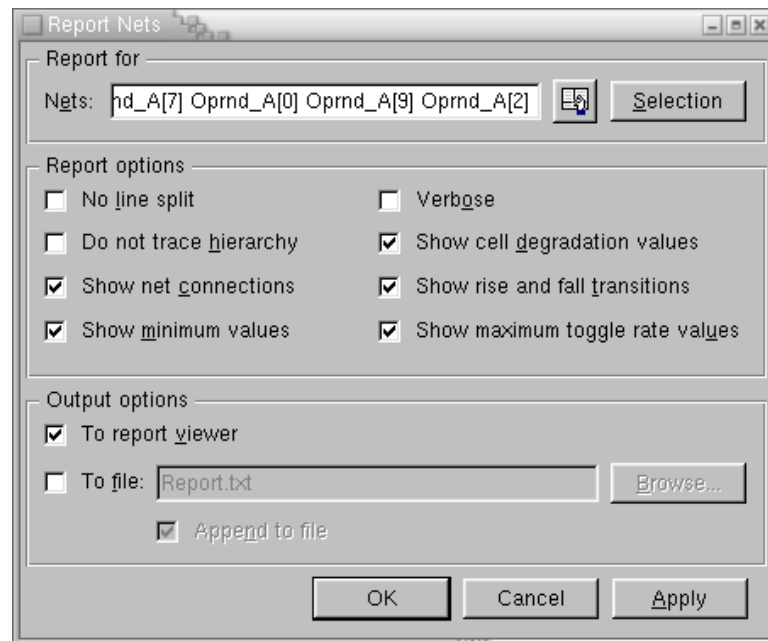


Figure 4-7

8. Report Clocks – This reports the properties of all clocks in the system. This includes clock rate (including duty cycle), and clock skew if there is any.

Design->Report Clocks

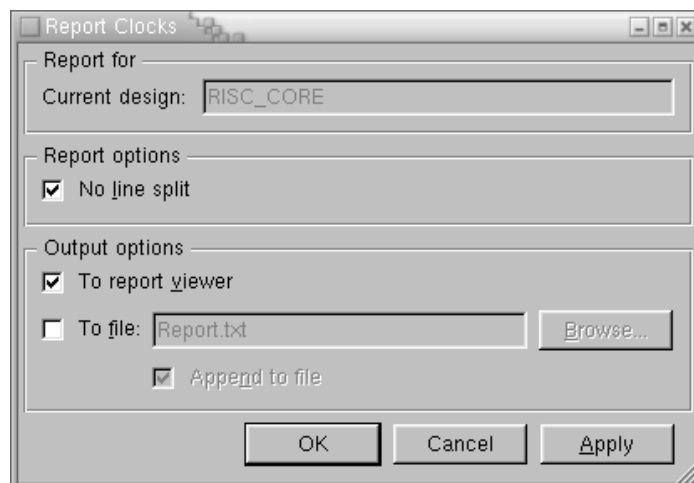


Figure 4-8

9. Report Area – This reports the final area of the design, showing sub values for the amount of combinatorial logic, sequential logic, and interconnect.

Design->Report Area

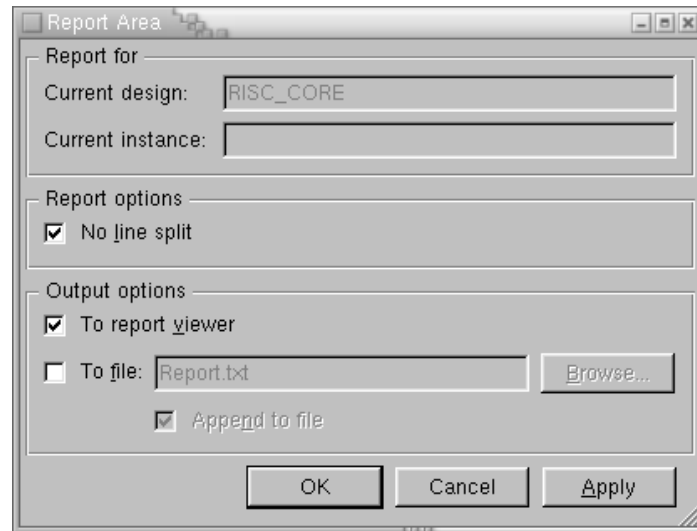


Figure 4-9

10. Report Compile Options – This reports the compile options used for each module in the design (specifically flattening, and structuring).

Design->Report Compile Options

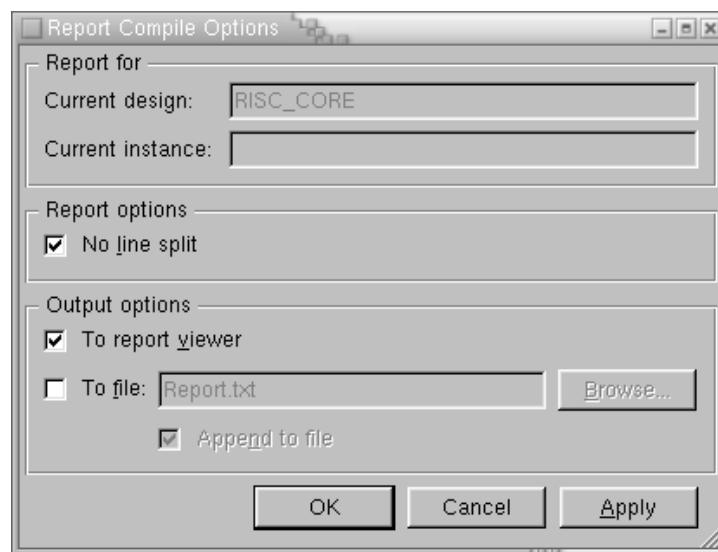


Figure 4-10

11. Report Power – This reports the amount of power consumed in the design. The report separates static and dynamic power. This option will not be necessary in ECE 551 but may provide an interesting comparison.

12. Path Slack

This report shows a histogram of paths in your design (basically all nets with a constrained timing path such as between the output of one FF and the input of another)

Timing->Path Slack

We will leave everything as it is in Figure 4-11 but note that there are additional settings we could use to change the paths that are included in the output histogram or change the appearance of the histogram.

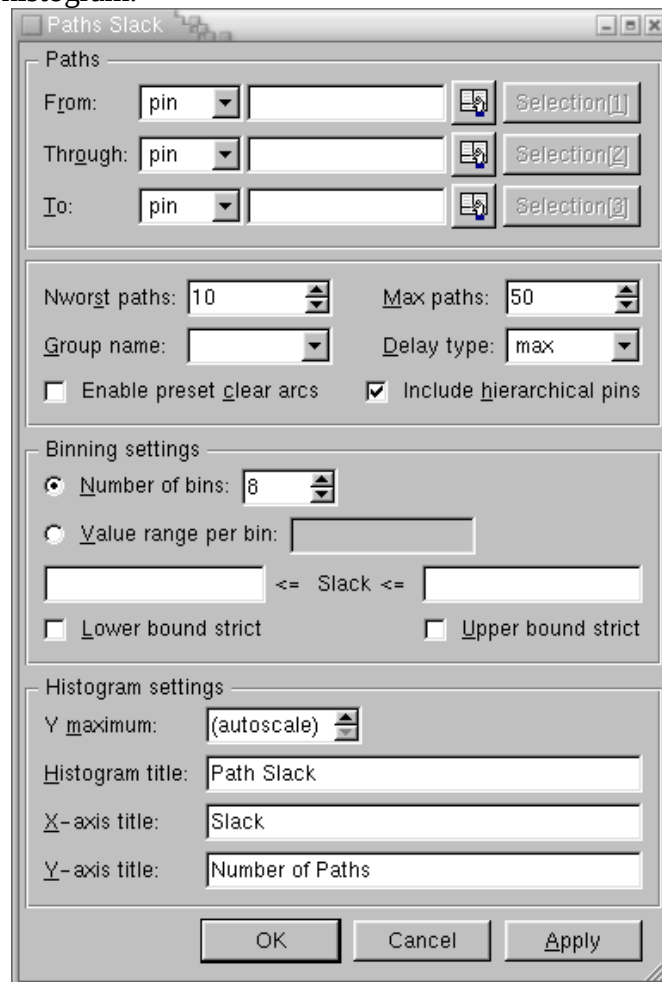


Figure 4-11

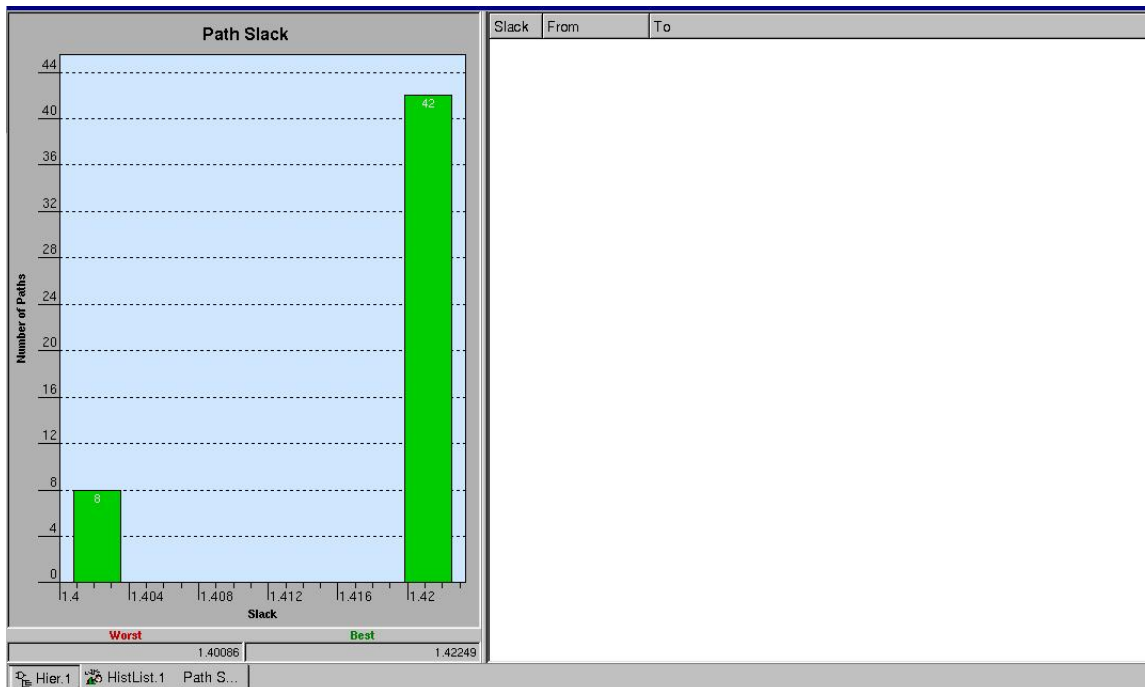


Figure 4-12

13. Endpoint Slack

This report is similar to path slack, except the only paths shown in this report are endpoints (the path ends at the output of a module or is unconstrained after the end of the path)

Timing->Endpoint Slack

Note that the choices available for endpoint slack are less than that of the path slack report. We will again leave the defaults for the tutorial.

Endpoint Slack

Delay type: max

Binning settings

☒ Number of bins: 8

☐ Value range per bin:

Slack <=

☐ Lower bound strict ☐ Upper bound strict

Histogram settings

Y maximum: (autoscale)

Histogram title: Endpoint Slack

X-axis title: Slack

Y-axis title: Number of Paths

OK Cancel Apply

Figure 4-13

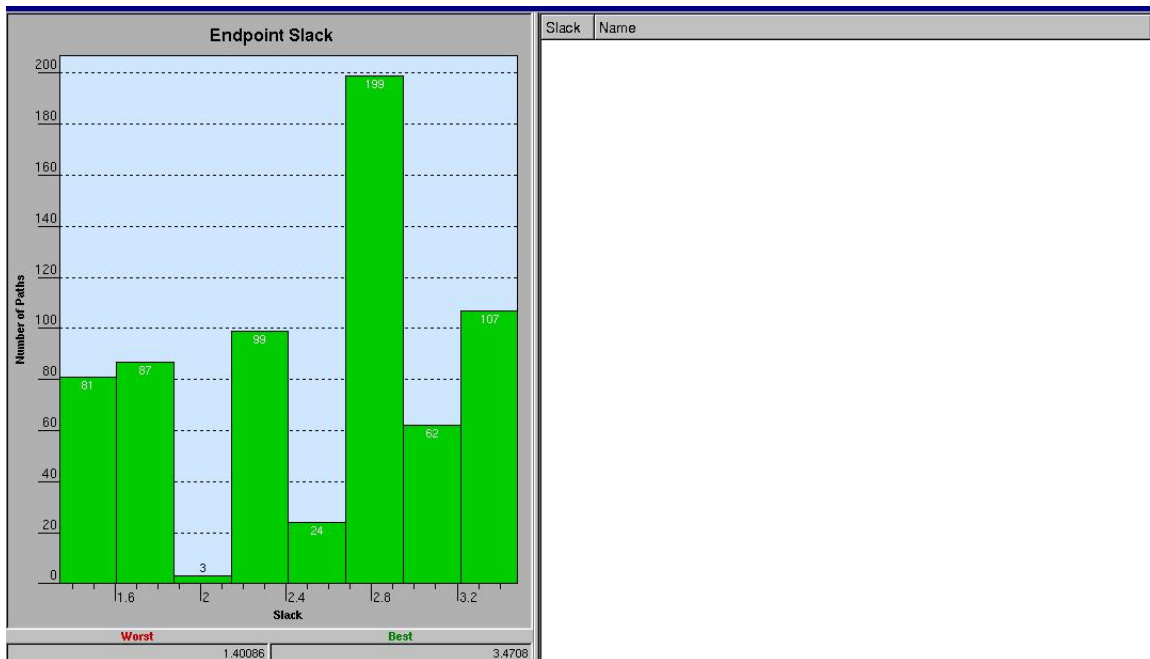


Figure 4-14

14. Report Timing Paths

Report timing paths is one of the most important reports for ECE 551 and in general. We will leave the report options at the defaults. When left at default, the report will give us the worst path delay in our entire design. If this report shows that we have met our clock speed constraints, then we know the entire design can run at the clock speed.

Timing->Report Timing Path...

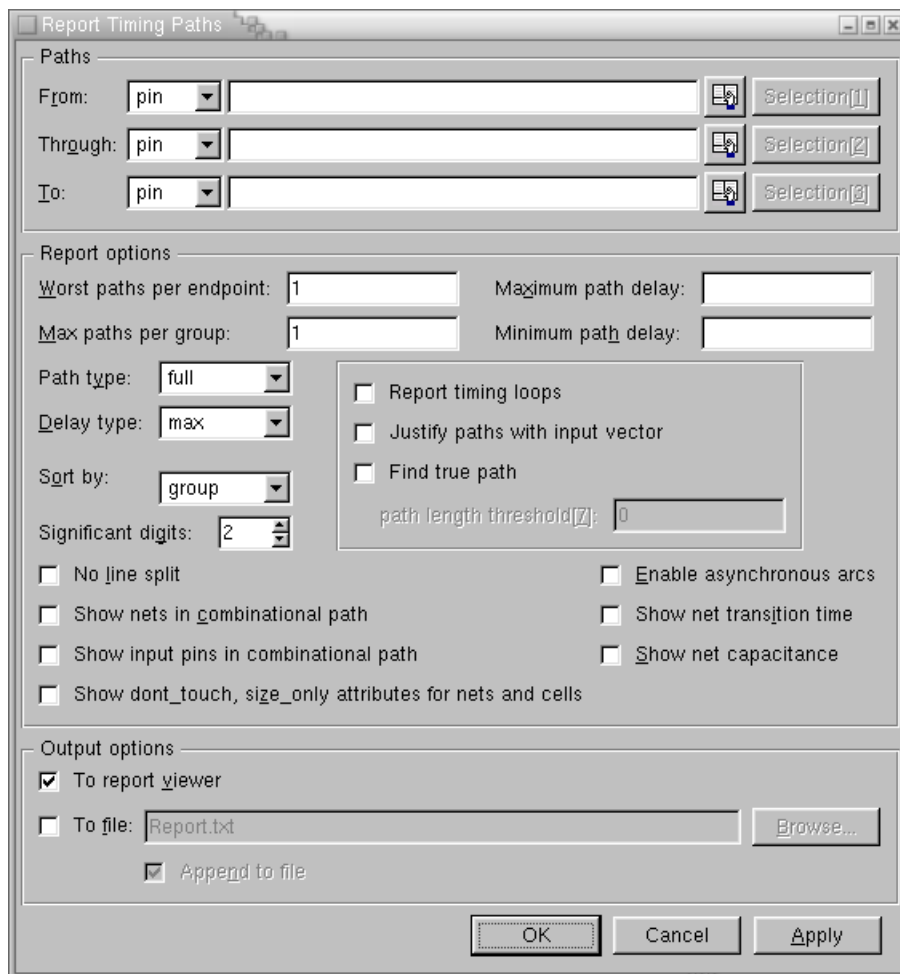


Figure 4-15

Because of the importance of this report, an example is included here rather than in Appendix C.

How to read this report: The first section starts at the output of a flip flop or primary input (Reset in this case) and lists a time (0 nS). The report then specifies each gate between this flip flop output and the d input of the flip flop at the endpoint (I_ALU/Zro_Flag_reg). It lists an incremental delay and total path delay at each step so that if you need to re-optimize the design, you know which types of gates to try and remove from the path. (In this case no gate or unit is particularly expensive but in some cases we see an obvious choice such as having two multipliers on the path). At the end a “data arrival time” is listed. In this example data arrival = 2.35 nS.

After that the “data required time is calculated. The data required time will be the clock period we were trying to achieve, with time subtracted to account for the setup time a DFF needs and potentially clock skew if we have specified any. In this example data required time = 3.75nS.

We then compare data required time to data arrival time and see that the clock speed constraint has been met and we have a slack (extra unused time) of 1.40nS. When listing our achievable clock rate, we can say our design has a maximum clock speed of (4nS (attempted) – 1.40nS (slack) = 2.60nS clock period). If we had not met the slack, the statement would say “slack (VIOLATED)” in which case we must add the time listed to our attempted clock rate. In general, if we do not meet our clock speed constraint, we should change the constraint and resynthesize, so that we only list achieved clock rate based upon a successful synthesis.

```
*****
Report : timing
        -path full
        -delay max
        -nworst 5
        -max_paths 5
        -sort_by group
Design : RISC_CORE
Version: Z-2007.03-SP3
Date   : Wed Oct  3 13:18:47 2007
*****
```

Operating Conditions: NOM Library: gflxp
Wire Load Model Mode: enclosed

Startpoint: Reset (input port clocked by Clk)
Endpoint: I_PRGRM_CNT_TOP/I_PRGRM_CNT/PCint_reg[0]
(rising edge-triggered flip-flop clocked by Clk)
Path Group: Clk
Path Type: max

Des/Clust/Port	Wire Load Model	Library
RISC_CORE	B1X1	gflxp
PRGRM_CNT	B0.1X0.1	gflxp

Point	Incr	Path
clock Clk (rise edge)	0.00	0.00
clock network delay (ideal)	0.00	0.00
input external delay	2.00	2.00 f
Reset (in)	0.00	2.00 f
I_PRGRM_CNT_TOP/Reset (PRGRM_CNT_TOP)	0.00	2.00 f
I_PRGRM_CNT_TOP/I_PRGRM_CNT/Reset (PRGRM_CNT)	0.00	2.00 f
I_PRGRM_CNT_TOP/I_PRGRM_CNT/U15/Z (NR2M1P)	0.05	2.05 r
I_PRGRM_CNT_TOP/I_PRGRM_CNT/U3/Z (NR2BNM1P)	0.20	2.25 r
I_PRGRM_CNT_TOP/I_PRGRM_CNT/U14/Z (A0I22M1P)	0.07	2.32 f
I_PRGRM_CNT_TOP/I_PRGRM_CNT/U23/Z (A021CNM1P)	0.03	2.35 r
I_PRGRM_CNT_TOP/I_PRGRM_CNT/PCint_reg[0]/D (FD1LQM1P)	0.00	2.35 r
data arrival time		2.35
clock Clk (rise edge)	4.00	4.00
clock network delay (ideal)	0.00	4.00
I_PRGRM_CNT_TOP/I_PRGRM_CNT/PCint_reg[0]/CP (FD1LQM1P)	0.00	4.00 r
library setup time	-0.25	3.75
data required time		3.75

data required time		3.75

data arrival time	-2.35

slack (MET)	1.40

15. Net Capacitance

Timing->Net Capacitance...

This option is not needed for ECE 551.

16. Check Timing

Timing->Check Timing...

This report performs a check of the timing constraints specified and gives potential errors. This report can be used for ECE 551 but is typically less accurate than post synthesis simulation in Modelsim, which will be covered later.

17. Report Clock Skew

Timing->Report Clock Skew...

This option is not needed for ECE 551.

18. Report Clock Tree

Timing->Report Clock Tree...

This option is not needed for ECE 551.

19. Report Path Group

Timing->Report Path Group...

This option is not needed for ECE 551.

20. Report Timing Constraints

Design->Report Constraints...

This report lists all timing constraints you have specified. This report tends to list more information than previous equivalent reports. The extra information is not needed for ECE 551.

Appendix A– Synopsys Code Directives

1. ``ifdef` – if the following macro is defined include the code
2. ``else` – code to include otherwise
3. ``endif` – the end of the if statement
4. ``define` – creates a macro
5. ``elsif` – combination of an else and if
6. ``ifndef` – if the following macro is not defined, include the code
7. ``include` – includes the specified file
8. ``undef` – undefines the macro (usually used in advance of redefinition)
9. ``undefineall` – undefines all macros
10. `//synopsys translate_on` – turns on the synthesis translation
11. `//synopsys translate_off` – turns off the synthesis translation
12. `//synopsys parallel_case` – specifies that the following case statement is purely parallel (i.e. only one case will execute, it is not possible for multiple of the cases to be true)
13. `//synopsys full_case` – specifies that the following case statement includes a statement for all of the possible combinations of the input select variables. This option should not be used in place of actually specifying all possibilities.
14. `//synopsys state_vector` – specifies that the following code is a state_vector
15. `//synopsys enum` – enumerates a list of variables and automatically assigns sequential numbers to the list
16. `//synopsys template` – specifies that the module is a template
17. `//synopsys dc_script_begin` – allows the inclusion of Design Compiler scripts within the code of your verilog
18. `//synopsys dc_script_end` – the end of the Design Compiler script

19.//synopsys map_to_module – specifies that the code be mapped to a particular module

20.//synopsys return_port_name – specifies the name of the return port (not necessary for normal code, this is an advanced feature for less common code styles)

Appendix B – Extra Optimization

1. Design Attributes

We may also specify design attributes, either on a module by module basis, or for the entire design at once.

1. Ungroup

Ungroup refers to the fact that this is a module. If we choose to ungroup, Design Vision will take all of the logic within the module and combine it with the logic at other levels of the design. This can obtain area benefits by possibly combining redundant logic.

2. Don't touch

Don't touch tells Design Vision to not alter the design as is. This is an option that can be used if the module is already synthesized and you do not want any changes made to the design. It is commonly used when a module is already optimized and we want to prevent changes that may result in a worse design

3. Boundary Optimization

Boundary Optimization is similar to ungroup except it only allows design vision to optimize the logic on the interface (Inputs and Outputs) of modules rather than allowing all internal logic to be possibly combined with other logic.

4. Disable wired logic(ECL)

This option refers to a style of connections which allows logic to be performed simply by connecting several wires together. We will never want wired logic for this course, so the option should always be checked.

5. Sequential elements

These options allow us to chose specific modules out of the library to be used within the design. This ability is an advanced feature that we will not use in this course.

6. Flatten logic

Flattening of logic takes multi-level logic and duplicates as many gates as possible to yield logic that is larger but potentially much faster.

a) Flatten Effort

This refers to how long design vision will allow the algorithm to run before moving on to the next portion. All algorithms of this type are non-deterministic (i.e. there is no exact solution, and no algorithm exists that can guarantee an optimal solution – also called NP-Complete). This effort refers to how long the algorithm is allowed to run without achieving positive results before we consider our solution as optimal.

b) Flatten minimize

This refers to whether we want the logic to try to minimize delay for only the most critical output, all of the outputs or none of the outputs.

c) Flatten phase

(i) Apply strategy – inverts the phase of the output during optimization

(ii) Don't apply – doesn't invert the phase of the output

7. Structure logic

Structuring determines whether structuring constraints are set in this design.

- a) Timing driven structuring – restructures the design to achieve better timing
- b) Boolean optimization – restructures the design to minimize the Boolean equations specified by the logic

Attributes->Optimization Directives->Design

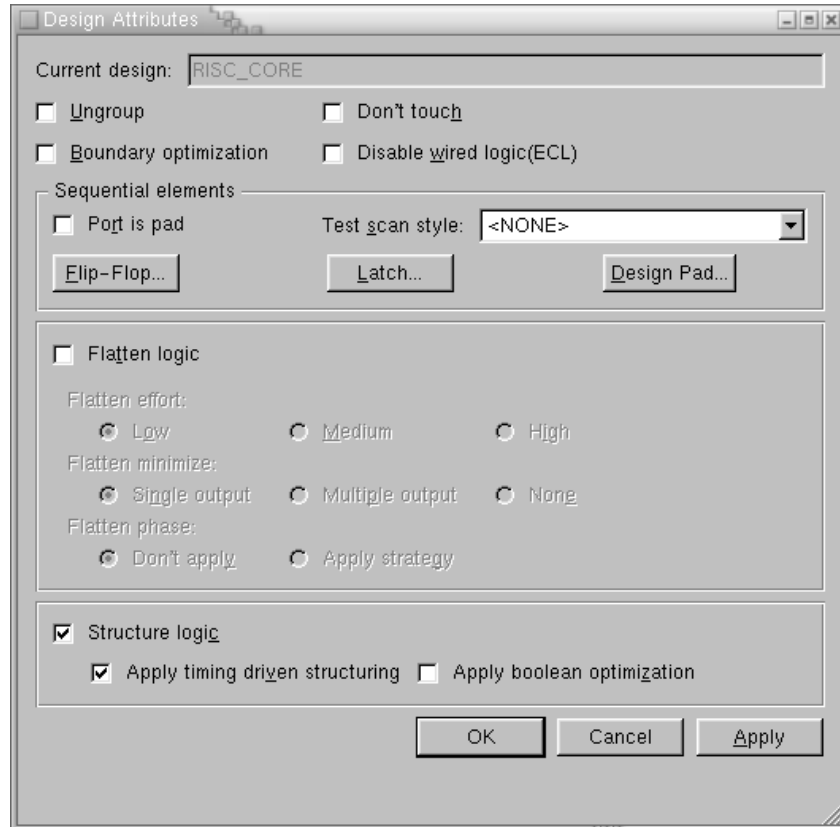
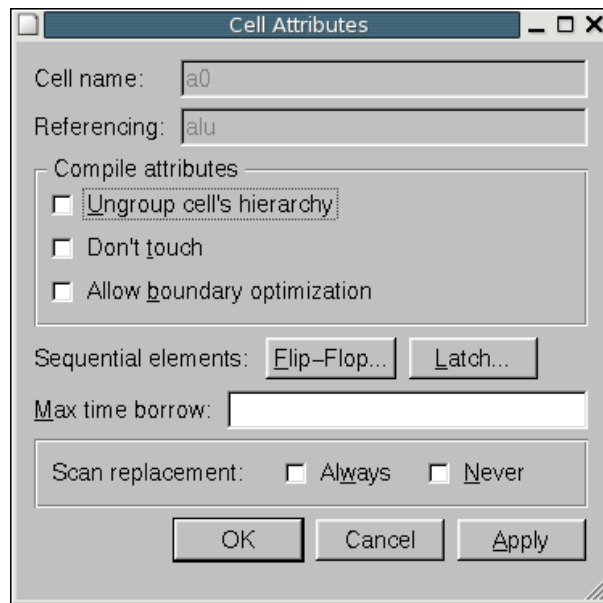


Figure 4-16 : Design Attributes Dialog

2. Cell Attributes

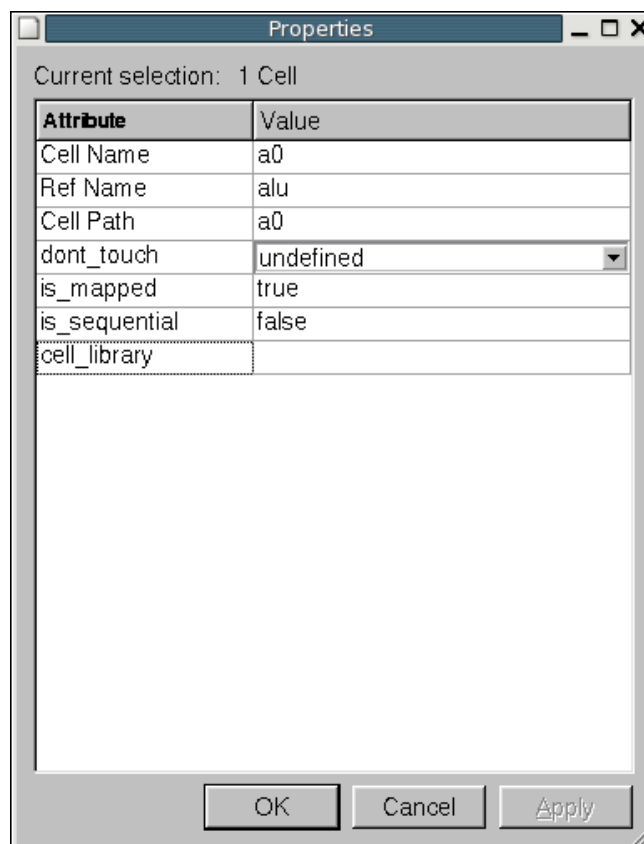
- a. Ungroup
- b. Don't Touch
- c. Allow Boundary Optimization
- d. Sequential Elements
- e. Max Time Element
- f. Scan Replacement



The 'Cell Attributes' dialog box is shown with the following fields and options:

- Cell name:** a0
- Referencing:** alu
- Compile attributes:**
 - ☐ Ungroup cell's hierarchy
 - ☐ Don't touch
 - ☐ Allow boundary optimization
- Sequential elements:** Flip-Flop... Latch...
- Max time borrow:** (empty text field)
- Scan replacement:** ☐ Always ☐ Never
- Buttons:** OK, Cancel, Apply

Figure 4-17 : Cell Attributes



The 'Properties' dialog box shows the current selection as '1 Cell'. It contains a table of attributes and their values:

Attribute	Value
Cell Name	a0
Ref Name	alu
Cell Path	a0
dont_touch	undefined
is_mapped	true
is_sequential	false
cell_library	

Buttons at the bottom: OK, Cancel, Apply

Figure 4-18 : Cell Properties

Appendix C - Reports Output

1. Report Design

Report : design

Design : RISC_CORE

Version: 2003.06

Date : Mon Sep 13 13:35:33 2004

Design allows ideal nets on clock nets.

Library(s) Used:

gflxp (File:
/usr/apps/eda/flexstream.3.3/lsi_fs_3.3/lib3p/synopsys/gflxp/gflxp_lsi_
wc.db)

Local Link Library:

{gflxp_lsi_wc.db, gflxio_lsi_wc.db}

Flip-Flop Types:

No flip-flop types specified.

Latch Types:

No latch types specified.

Operating Conditions:

Name	Library	Calc_mode	Process	Temp	Volt	Interconnect
------	---------	-----------	---------	------	------	--------------

Model

LSI_WC	gflxp		1.32	115.00	1.08	balanced_tree
--------	-------	--	------	--------	------	---------------

Wire Loading Model:

Selected manually by the user.

Name	:	B1X1 *
Location	:	gflxp
Resistance	:	0.000569
Capacitance	:	0.000167
Area	:	0.095862
Slope	:	54.8
Fanout	Length	Points Average Cap Std Deviation

1	24.80
2	81.00
3	137.30
4	193.50
5	249.70
6	306.00
7	362.20
8	418.50
9	474.70
10	531.00

Wire Loading Model Mode: enclosed.

Timing Ranges:

No timing ranges specified.

Pin Input Delays:

None specified.

Pin Output Delays:

None specified.

Disabled Timing Arcs:

No arcs disabled.

Required Licenses:

None Required

Design Parameters:

None specified.

2. Report Design Hierarchy

Report : hierarchy

Design : RISC_CORE

Version: 2003.06

Date : Mon Sep 13 13:36:29 2004

RISC_CORE

ALU

ALU_DW01_addsub_16_0

AND2M1P	gflxp
A0I21M6P	gflxp
ENFM1P	gflxp
ENFM2P	gflxp
E0FM1P	gflxp
E0FM2P	gflxp
N1M1P	gflxp
N1M2P	gflxp
ND2BNM1P	gflxp
ND2BNM2P	gflxp
ND2M1P	gflxp
ND2M2P	gflxp
0A21M1P	gflxp
0AI21M1P	gflxp
0AI21M2P	gflxp
0AI21M4P	gflxp

ALU_DW01_addsub_16_2

A0I21M1P	gflxp
A0I21M2P	gflxp
ENFM1P	gflxp
ENFM2P	gflxp
E0FM1P	gflxp
E0FM2P	gflxp
N1M1P	gflxp

N1M2P	gflxp
ND2BNM1P	gflxp
ND2BNM2P	gflxp
ND2M1P	gflxp
ND2M2P	gflxp
NR2BNM1P	gflxp
NR2BNM2P	gflxp
NR2M1P	gflxp
NR2M2P	gflxp
NR2M3P	gflxp
OA21M1P	gflxp
OAI21M1P	gflxp
OAI21M2P	gflxp
AND2M1P	gflxp
AND2M2P	gflxp
A021CNM1P	gflxp
A021CNM2P	gflxp
A021M1P	gflxp
A022M1P	gflxp
A0211M1P	gflxp
E0FM1P	gflxp
FD1LQM1P	gflxp
FD1SLQM1P	gflxp
MUX21HFM2P	gflxp
MUX21HM1P	gflxp
N1M1P	gflxp
N1M2P	gflxp
N1M4P	gflxp
ND3CNM1P	gflxp
ND3CNM2P	gflxp
ND8M1P	gflxp
NR2M1P	gflxp
NR3M1P	gflxp
NR8M1P	gflxp
OA21M1P	gflxp
OR2M1P	gflxp
OR2M2P	gflxp
OR2M4P	gflxp
OR2M8P	gflxp
OR2M10P	gflxp
OR3M1P	gflxp
OR3M2P	gflxp
OR3M8P	gflxp
BUFM1P	gflxp
BUFM2P	gflxp
CONTROL	
AND2M1P	gflxp
AND2M4P	gflxp
AND3M1P	gflxp
AND3M4P	gflxp
A021CNM1P	gflxp
A0I211M1P	gflxp
BUFM10P	gflxp
E0FM1P	gflxp
FD1QM1P	gflxp
FD1SQM1P	gflxp
FD1SQM3P	gflxp

MUX21HM1P	gflxp
N1M1P	gflxp
ND5M1P	gflxp
ND6M2P	gflxp
NR2I1M12P	gflxp
NR5M1P	gflxp
OR2M1P	gflxp
DATA_PATH	
AND2M1P	gflxp
A022M1P	gflxp
FD1LQM1P	gflxp
FD1SLQM1P	gflxp
FD1SLQM3P	gflxp
MUX21HM1P	gflxp
MUX21HM2P	gflxp
N1M1P	gflxp
ND2BNM1P	gflxp
ND4CDNM1P	gflxp
NR2M1P	gflxp
NR2M2P	gflxp
NR4M1P	gflxp
OR2M2P	gflxp
OR3M1P	gflxp
INSTRN_LAT	
FD1LQM1P	gflxp
FD1LQM3P	gflxp
PRGRM_CNT_TOP	
PRGRM_CNT	
A0222M2P	gflxp
FD1LQM1P	gflxp
FD1LQM3P	gflxp
N1M1P	gflxp
NR2M1P	gflxp
NR3M2P	gflxp
OR2M1P	gflxp
OR3M1P	gflxp
PRGRM_CNT_DW01_inc_8_0	
E0FM1P	gflxp
HA1M2P	gflxp
N1M1P	gflxp
PRGRM_DECODE	
AND2M1P	gflxp
AND3M1P	gflxp
AND4M1P	gflxp
E0FM1P	gflxp
MUX21HM1P	gflxp
MUX31HM2P	gflxp
N1M1P	gflxp
ND2M1P	gflxp
ND3BCNM1P	gflxp
ND4CDNM1P	gflxp
NR6M2P	gflxp
OR2M1P	gflxp
OR3M1P	gflxp
PRGRM_FSM	
AND2M1P	gflxp
AND3M1P	gflxp

FD1QM1P	gflxp
MUX21HM1P	gflxp
N1M1P	gflxp
NR2M1P	gflxp
REG_FILE	
A022M1P	gflxp
FD1LQM1P	gflxp
N1M1P	gflxp
NR2M2P	gflxp
OAI2222M1P	gflxp
OR2M1P	gflxp
OR2M8P	gflxp
STACK_TOP	
STACK_FSM	
AND2M1P	gflxp
AND3M1P	gflxp
AND4M1P	gflxp
A021CNM1P	gflxp
A0211M1P	gflxp
ENFM1P	gflxp
E0FM1P	gflxp
FD1LQM3P	gflxp
FD1QM1P	gflxp
FD1QM3P	gflxp
MUX21HM1P	gflxp
N1M1P	gflxp
NR2BNM1P	gflxp
NR2M1P	gflxp
NR3M1P	gflxp
OA21M1P	gflxp
OR2M1P	gflxp
OR3M1P	gflxp
STACK_MEM_0	
BUFM3P	gflxp
ENFM1P	gflxp
E0FM1P	gflxp
FD1LQM1P	gflxp
MUX21HM1P	gflxp
MUX21LM1P	gflxp
N1M1P	gflxp
ND2M1P	gflxp
NR2M1P	gflxp
NR3M1P	gflxp
NR3M2P	gflxp
OA2222M1P	gflxp
OR3M1P	gflxp
STACK_MEM_1	
ENFM1P	gflxp
E0FM1P	gflxp
FD1LQM1P	gflxp
MUX21HM1P	gflxp
MUX21LM1P	gflxp
N1M1P	gflxp
ND2M1P	gflxp
NR2M1P	gflxp
NR3M2P	gflxp
OA2222M1P	gflxp

OR3M1P	gflxp
STACK_MEM_2	
ENFM1P	gflxp
E0FM1P	gflxp
FD1LQM1P	gflxp
MUX21HM1P	gflxp
MUX21LM1P	gflxp
N1M1P	gflxp
ND2M1P	gflxp
NR2M1P	gflxp
NR3M2P	gflxp
OA2222M1P	gflxp
OR3M1P	gflxp

3. Report Reference

 Report : reference
 Design : RISC_CORE
 Version: 2003.06
 Date : Mon Sep 13 13:37:48 2004

Attributes:

b - black box (unknown)
 bo - allows boundary optimization
 d - dont_touch
 mo - map_only
 h - hierarchical
 n - noncombinational
 r - removable
 s - synthetic operator
 u - contains unmapped logic

Reference	Library	Unit Area	Count	Total Area	Attributes
ALU		4401.900391	1	4401.900391	h, n
BUFM1P	gflxp	4.001200	33	132.039612	
BUFM2P	gflxp	5.001900	1	5.001900	
CONTROL		331.057709	1	331.057709	h, n
DATA_PATH		1620.130859	1	1620.130859	h, n
INSTRN_LAT		1921.102661	1	1921.102661	h, n
PRGRM_CNT_TOP		735.097717	1	735.097717	h, n
REG_FILE		3522.355469	1	3522.355469	h, n
STACK_TOP		5975.694824	1	5975.694824	h, n
Total 9 references				18644.380859	

4. Report Wire Loads

Report : wire loads

Design : RISC_CORE

Version: 2003.06

Date : Mon Sep 13 13:58:25 2004

Wire load model: B0.1X0.1

Location : ALU_DW01_addsub_16_2 (design)

Resistance : 0.000569

Capacitance : 0.000167

Area : 0.095862

Slope : 8.9

Fanout	Length	Points	Average Cap	Standard Deviation	% Standard Deviation
--------	--------	--------	----------------	-----------------------	-------------------------

1	0.50				
2	9.60				
3	18.80				
4	27.90				
5	37.10				
6	46.20				
7	55.40				
8	64.50				
9	73.70				
10	82.90				

Wire load model: B0.2X0.2

Location : ALU (design)

Resistance : 0.000569

Capacitance : 0.000167

Area : 0.095862

Slope : 18.4

Fanout	Length	Points	Average Cap	Standard Deviation	% Standard Deviation
--------	--------	--------	----------------	-----------------------	-------------------------

1	5.60				
2	24.40				
3	43.30				
4	62.20				
5	81.00				
6	99.80				
7	118.70				
8	137.50				
9	156.40				
10	175.20				

Wire load model: B1X1

Location : RISC_CORE (design)

Resistance : 0.000569

Capacitance : 0.000167

Area : 0.095862

Slope : 54.8

Fanout	Length	Points	Average Cap	Standard Deviation	% Standard Deviation
--------	--------	--------	----------------	-----------------------	-------------------------

```

-----
1      24.80
2      81.00
3     137.30
4     193.50
5     249.70
6     306.00
7     362.20
8     418.50
9     474.70
10    531.00
-----

```

5. Report Ports

Report : port

-verbose

Design : RISC_CORE

Version: 2003.06

Date : Mon Sep 13 13:38:53 2004

Port	Dir	Pin Load	Wire Load	Max Trans	Max Cap	Connection Class	Attrs

Xecutng_Instrn[2]							
out		0.0000	0.0000	--	--	--	
Instrn[6]	in	0.0000	0.0000	--	--	--	
PSW[6]	out	0.0000	0.0000	--	--	--	
PSW[9]	out	0.0000	0.0000	--	--	--	
Xecutng_Instrn[25]							
out		0.0000	0.0000	--	--	--	
Instrn[29]	in	0.0000	0.0000	--	--	--	
RESULT_DATA[11]							
out		0.0000	0.0000	--	--	--	
Xecutng_Instrn[18]							
out		0.0000	0.0000	--	--	--	
Instrn[22]	in	0.0000	0.0000	--	--	--	
RESULT_DATA[4]	out	0.0000	0.0000	--	--	--	
Xecutng_Instrn[11]							
out		0.0000	0.0000	--	--	--	
Instrn[15]	in	0.0000	0.0000	--	--	--	
Xecutng_Instrn[4]							
out		0.0000	0.0000	--	--	--	
Instrn[8]	in	0.0000	0.0000	--	--	--	
Instrn[1]	in	0.0000	0.0000	--	--	--	
PSW[1]	out	0.0000	0.0000	--	--	--	
Xecutng_Instrn[27]							
out		0.0000	0.0000	--	--	--	
Instrn[31]	in	0.0000	0.0000	--	--	--	
RESULT_DATA[13]							
out		0.0000	0.0000	--	--	--	
Xecutng_Instrn[20]							
out		0.0000	0.0000	--	--	--	

Instrn[24]	in	0.0000	0.0000	--	--	--
RESULT_DATA[6]	out	0.0000	0.0000	--	--	--
Xecutng_Instrn[13]						
	out	0.0000	0.0000	--	--	--
Instrn[17]	in	0.0000	0.0000	--	--	--
Xecutng_Instrn[6]						
	out	0.0000	0.0000	--	--	--
Instrn[10]	in	0.0000	0.0000	--	--	--
Instrn[3]	in	0.0000	0.0000	--	--	--
PSW[3]	out	0.0000	0.0000	--	--	--
Reset	in	0.0000	0.0000	--	--	--
Xecutng_Instrn[29]						
	out	0.0000	0.0000	--	--	--
RESULT_DATA[15]						
	out	0.0000	0.0000	--	--	--
Xecutng_Instrn[22]						
	out	0.0000	0.0000	--	--	--
Instrn[26]	in	0.0000	0.0000	--	--	--
RESULT_DATA[8]	out	0.0000	0.0000	--	--	--
Xecutng_Instrn[15]						
	out	0.0000	0.0000	--	--	--
Instrn[19]	in	0.0000	0.0000	--	--	--
RESULT_DATA[1]	out	0.0000	0.0000	--	--	--
Xecutng_Instrn[8]						
	out	0.0000	0.0000	--	--	--
Instrn[12]	in	0.0000	0.0000	--	--	--
Xecutng_Instrn[1]						
	out	0.0000	0.0000	--	--	--
Instrn[5]	in	0.0000	0.0000	--	--	--
PSW[5]	out	0.0000	0.0000	--	--	--
Clk	in	0.0000	0.0000	--	--	--
PSW[8]	out	0.0000	0.0000	--	--	--
Xecutng_Instrn[31]						
	out	0.0000	0.0000	--	--	--
Rd_Instr	out	0.0000	0.0000	--	--	--
Xecutng_Instrn[24]						
	out	0.0000	0.0000	--	--	--
Instrn[28]	in	0.0000	0.0000	--	--	--
RESULT_DATA[10]						
	out	0.0000	0.0000	--	--	--
Xecutng_Instrn[17]						
	out	0.0000	0.0000	--	--	--
Instrn[21]	in	0.0000	0.0000	--	--	--
RESULT_DATA[3]	out	0.0000	0.0000	--	--	--
Xecutng_Instrn[10]						
	out	0.0000	0.0000	--	--	--
Instrn[14]	in	0.0000	0.0000	--	--	--
STACK_FULL	out	0.0000	0.0000	--	--	--
Xecutng_Instrn[3]						
	out	0.0000	0.0000	--	--	--
Instrn[7]	in	0.0000	0.0000	--	--	--
PSW[7]	out	0.0000	0.0000	--	--	--
PSW[10]	out	0.0000	0.0000	--	--	--
Instrn[0]	in	0.0000	0.0000	--	--	--
PSW[0]	out	0.0000	0.0000	--	--	--
Xecutng_Instrn[26]						
	out	0.0000	0.0000	--	--	--

Instrn[30]	in	0.0000	0.0000	--	--	--
RESULT_DATA[12]						
	out	0.0000	0.0000	--	--	--
Xecutng_Instrn[19]						
	out	0.0000	0.0000	--	--	--
Instrn[23]	in	0.0000	0.0000	--	--	--
RESULT_DATA[5]	out	0.0000	0.0000	--	--	--
Xecutng_Instrn[12]						
	out	0.0000	0.0000	--	--	--
Instrn[16]	in	0.0000	0.0000	--	--	--
OUT_VALID	out	0.0000	0.0000	--	--	--
Xecutng_Instrn[5]						
	out	0.0000	0.0000	--	--	--
Instrn[9]	in	0.0000	0.0000	--	--	--
EndOfInstrn	out	0.0000	0.0000	--	--	--
Instrn[2]	in	0.0000	0.0000	--	--	--
PSW[2]	out	0.0000	0.0000	--	--	--
Xecutng_Instrn[28]						
	out	0.0000	0.0000	--	--	--
RESULT_DATA[14]						
	out	0.0000	0.0000	--	--	--
Xecutng_Instrn[21]						
	out	0.0000	0.0000	--	--	--
Instrn[25]	in	0.0000	0.0000	--	--	--
RESULT_DATA[7]	out	0.0000	0.0000	--	--	--
Xecutng_Instrn[14]						
	out	0.0000	0.0000	--	--	--
Instrn[18]	in	0.0000	0.0000	--	--	--
RESULT_DATA[0]	out	0.0000	0.0000	--	--	--
Xecutng_Instrn[7]						
	out	0.0000	0.0000	--	--	--
Instrn[11]	in	0.0000	0.0000	--	--	--
Xecutng_Instrn[0]						
	out	0.0000	0.0000	--	--	--
Instrn[4]	in	0.0000	0.0000	--	--	--
PSW[4]	out	0.0000	0.0000	--	--	--
Xecutng_Instrn[30]						
	out	0.0000	0.0000	--	--	--
Xecutng_Instrn[23]						
	out	0.0000	0.0000	--	--	--
Instrn[27]	in	0.0000	0.0000	--	--	--
RESULT_DATA[9]	out	0.0000	0.0000	--	--	--
Xecutng_Instrn[16]						
	out	0.0000	0.0000	--	--	--
Instrn[20]	in	0.0000	0.0000	--	--	--
RESULT_DATA[2]	out	0.0000	0.0000	--	--	--
Xecutng_Instrn[9]						
	out	0.0000	0.0000	--	--	--
Instrn[13]	in	0.0000	0.0000	--	--	--
Port	External Number Points	Max Wireload Model	Min Wireload Model		Min Pin Load	Min Wire Load

Xecutng_Instrn[2]	1	--	--		--	--

Instrn[6]	1	--	--	--	--
PSW[6]	1	--	--	--	--
PSW[9]	1	--	--	--	--
Xecutng_Instrn[25]	1	--	--	--	--
Instrn[29]	1	--	--	--	--
RESULT_DATA[11]	1	--	--	--	--
Xecutng_Instrn[18]	1	--	--	--	--
Instrn[22]	1	--	--	--	--
RESULT_DATA[4]	1	--	--	--	--
Xecutng_Instrn[11]	1	--	--	--	--
Instrn[15]	1	--	--	--	--
Xecutng_Instrn[4]	1	--	--	--	--
Instrn[8]	1	--	--	--	--
Instrn[1]	1	--	--	--	--
PSW[1]	1	--	--	--	--
Xecutng_Instrn[27]	1	--	--	--	--
Instrn[31]	1	--	--	--	--
RESULT_DATA[13]	1	--	--	--	--
Xecutng_Instrn[20]	1	--	--	--	--
Instrn[24]	1	--	--	--	--
RESULT_DATA[6]	1	--	--	--	--
Xecutng_Instrn[13]	1	--	--	--	--
Instrn[17]	1	--	--	--	--
Xecutng_Instrn[6]	1	--	--	--	--
Instrn[10]	1	--	--	--	--
Instrn[3]	1	--	--	--	--
PSW[3]	1	--	--	--	--
Reset	1	--	--	--	--
Xecutng_Instrn[29]	1	--	--	--	--
RESULT_DATA[15]	1	--	--	--	--
Xecutng_Instrn[22]	1	--	--	--	--
Instrn[26]	1	--	--	--	--
RESULT_DATA[8]	1	--	--	--	--
Xecutng_Instrn[15]	1	--	--	--	--
Instrn[19]	1	--	--	--	--
RESULT_DATA[1]	1	--	--	--	--
Xecutng_Instrn[8]	1	--	--	--	--
Instrn[12]	1	--	--	--	--

Xecutng_Instrn[1]	1	--	--	--	--
Instrn[5]	1	--	--	--	--
PSW[5]	1	--	--	--	--
Clk	1	--	--	--	--
PSW[8]	1	--	--	--	--
Xecutng_Instrn[31]	1	--	--	--	--
Rd_Instr	1	--	--	--	--
Xecutng_Instrn[24]	1	--	--	--	--
Instrn[28]	1	--	--	--	--
RESULT_DATA[10]	1	--	--	--	--
Xecutng_Instrn[17]	1	--	--	--	--
Instrn[21]	1	--	--	--	--
RESULT_DATA[3]	1	--	--	--	--
Xecutng_Instrn[10]	1	--	--	--	--
Instrn[14]	1	--	--	--	--
STACK_FULL	1	--	--	--	--
Xecutng_Instrn[3]	1	--	--	--	--
Instrn[7]	1	--	--	--	--
PSW[7]	1	--	--	--	--
PSW[10]	1	--	--	--	--
Instrn[0]	1	--	--	--	--
PSW[0]	1	--	--	--	--
Xecutng_Instrn[26]	1	--	--	--	--
Instrn[30]	1	--	--	--	--
RESULT_DATA[12]	1	--	--	--	--
Xecutng_Instrn[19]	1	--	--	--	--
Instrn[23]	1	--	--	--	--
RESULT_DATA[5]	1	--	--	--	--
Xecutng_Instrn[12]	1	--	--	--	--
Instrn[16]	1	--	--	--	--
OUT_VALID	1	--	--	--	--
Xecutng_Instrn[5]	1	--	--	--	--
Instrn[9]	1	--	--	--	--
EndOfInstrn	1	--	--	--	--
Instrn[2]	1	--	--	--	--
PSW[2]	1	--	--	--	--
Xecutng_Instrn[28]	1	--	--	--	--
RESULT_DATA[14]	1	--	--	--	--
Xecutng_Instrn[21]	1	--	--	--	--
Instrn[25]	1	--	--	--	--

RESULT_DATA[7]	1	--	--	--	--
Xecutng_Instrn[14]	1	--	--	--	--
Instrn[18]	1	--	--	--	--
RESULT_DATA[0]	1	--	--	--	--
Xecutng_Instrn[7]	1	--	--	--	--
Instrn[11]	1	--	--	--	--
Xecutng_Instrn[0]	1	--	--	--	--
Instrn[4]	1	--	--	--	--
PSW[4]	1	--	--	--	--
Xecutng_Instrn[30]	1	--	--	--	--
Xecutng_Instrn[23]	1	--	--	--	--
Instrn[27]	1	--	--	--	--
RESULT_DATA[9]	1	--	--	--	--
Xecutng_Instrn[16]	1	--	--	--	--
Instrn[20]	1	--	--	--	--
RESULT_DATA[2]	1	--	--	--	--
Xecutng_Instrn[9]	1	--	--	--	--
Instrn[13]	1	--	--	--	--

Input Port	Input Delay		Max		Related Clock	Max Fanout
	Min Rise	Min Fall	Max Rise	Max Fall		
Instrn[6]	2.00	2.00	2.00	2.00	Clk	--
Instrn[29]	2.00	2.00	2.00	2.00	Clk	--
Instrn[22]	2.00	2.00	2.00	2.00	Clk	--
Instrn[15]	2.00	2.00	2.00	2.00	Clk	--
Instrn[8]	2.00	2.00	2.00	2.00	Clk	--
Instrn[1]	2.00	2.00	2.00	2.00	Clk	--
Instrn[31]	2.00	2.00	2.00	2.00	Clk	--
Instrn[24]	2.00	2.00	2.00	2.00	Clk	--
Instrn[17]	2.00	2.00	2.00	2.00	Clk	--
Instrn[10]	2.00	2.00	2.00	2.00	Clk	--
Instrn[3]	2.00	2.00	2.00	2.00	Clk	--
Reset	2.00	2.00	2.00	2.00	Clk	--
Instrn[26]	2.00	2.00	2.00	2.00	Clk	--
Instrn[19]	2.00	2.00	2.00	2.00	Clk	--
Instrn[12]	2.00	2.00	2.00	2.00	Clk	--
Instrn[5]	2.00	2.00	2.00	2.00	Clk	--
Clk	--	--	--	--	--	--
Instrn[28]	2.00	2.00	2.00	2.00	Clk	--
Instrn[21]	2.00	2.00	2.00	2.00	Clk	--
Instrn[14]	2.00	2.00	2.00	2.00	Clk	--
Instrn[7]	2.00	2.00	2.00	2.00	Clk	--
Instrn[0]	2.00	2.00	2.00	2.00	Clk	--
Instrn[30]	2.00	2.00	2.00	2.00	Clk	--
Instrn[23]	2.00	2.00	2.00	2.00	Clk	--

Instrn[16]	2.00	2.00	2.00	2.00	Clk	--
Instrn[9]	2.00	2.00	2.00	2.00	Clk	--
Instrn[2]	2.00	2.00	2.00	2.00	Clk	--
Instrn[25]	2.00	2.00	2.00	2.00	Clk	--
Instrn[18]	2.00	2.00	2.00	2.00	Clk	--
Instrn[11]	2.00	2.00	2.00	2.00	Clk	--
Instrn[4]	2.00	2.00	2.00	2.00	Clk	--
Instrn[27]	2.00	2.00	2.00	2.00	Clk	--
Instrn[20]	2.00	2.00	2.00	2.00	Clk	--
Instrn[13]	2.00	2.00	2.00	2.00	Clk	--

Driving Cell

Input Port	Rise	Fall	Mult	Attrs
Instrn[6]	gflxio/DDRVL33/Z (A)			
		gflxio/DDRVL33/Z (A)	--	
Instrn[29]	gflxio/DDRVL33/Z (A)			
		gflxio/DDRVL33/Z (A)	--	
Instrn[22]	gflxio/DDRVL33/Z (A)			
		gflxio/DDRVL33/Z (A)	--	
Instrn[15]	gflxio/DDRVL33/Z (A)			
		gflxio/DDRVL33/Z (A)	--	
Instrn[8]	gflxio/DDRVL33/Z (A)			
		gflxio/DDRVL33/Z (A)	--	
Instrn[1]	gflxio/DDRVL33/Z (A)			
		gflxio/DDRVL33/Z (A)	--	
Instrn[31]	gflxio/DDRVL33/Z (A)			
		gflxio/DDRVL33/Z (A)	--	
Instrn[24]	gflxio/DDRVL33/Z (A)			
		gflxio/DDRVL33/Z (A)	--	
Instrn[17]	gflxio/DDRVL33/Z (A)			
		gflxio/DDRVL33/Z (A)	--	
Instrn[10]	gflxio/DDRVL33/Z (A)			
		gflxio/DDRVL33/Z (A)	--	
Instrn[3]	gflxio/DDRVL33/Z (A)			
		gflxio/DDRVL33/Z (A)	--	
Reset	gflxio/DDRVL33/Z (A)			
		gflxio/DDRVL33/Z (A)	--	
Instrn[26]	gflxio/DDRVL33/Z (A)			
		gflxio/DDRVL33/Z (A)	--	
Instrn[19]	gflxio/DDRVL33/Z (A)			
		gflxio/DDRVL33/Z (A)	--	
Instrn[12]	gflxio/DDRVL33/Z (A)			
		gflxio/DDRVL33/Z (A)	--	

Instrn[5]	gflxio/DDRVL33/Z (A)				--
	gflxio/DDRVL33/Z (A)				--
Instrn[28]	gflxio/DDRVL33/Z (A)				--
	gflxio/DDRVL33/Z (A)				--
Instrn[21]	gflxio/DDRVL33/Z (A)				--
	gflxio/DDRVL33/Z (A)				--
Instrn[14]	gflxio/DDRVL33/Z (A)				--
	gflxio/DDRVL33/Z (A)				--
Instrn[7]	gflxio/DDRVL33/Z (A)				--
	gflxio/DDRVL33/Z (A)				--
Instrn[0]	gflxio/DDRVL33/Z (A)				--
	gflxio/DDRVL33/Z (A)				--
Instrn[30]	gflxio/DDRVL33/Z (A)				--
	gflxio/DDRVL33/Z (A)				--
Instrn[23]	gflxio/DDRVL33/Z (A)				--
	gflxio/DDRVL33/Z (A)				--
Instrn[16]	gflxio/DDRVL33/Z (A)				--
	gflxio/DDRVL33/Z (A)				--
Instrn[9]	gflxio/DDRVL33/Z (A)				--
	gflxio/DDRVL33/Z (A)				--
Instrn[2]	gflxio/DDRVL33/Z (A)				--
	gflxio/DDRVL33/Z (A)				--
Instrn[25]	gflxio/DDRVL33/Z (A)				--
	gflxio/DDRVL33/Z (A)				--
Instrn[18]	gflxio/DDRVL33/Z (A)				--
	gflxio/DDRVL33/Z (A)				--
Instrn[11]	gflxio/DDRVL33/Z (A)				--
	gflxio/DDRVL33/Z (A)				--
Instrn[4]	gflxio/DDRVL33/Z (A)				--
	gflxio/DDRVL33/Z (A)				--
Instrn[27]	gflxio/DDRVL33/Z (A)				--
	gflxio/DDRVL33/Z (A)				--
Instrn[20]	gflxio/DDRVL33/Z (A)				--
	gflxio/DDRVL33/Z (A)				--
Instrn[13]	gflxio/DDRVL33/Z (A)				--
	gflxio/DDRVL33/Z (A)				--
Cell	Max Drive	Min Drive	Resistance	Min	Min

Input Port Deg	Rise	Fall	Rise	Fall	Max	Min	Cap	Fanout

Instrn[6]	--	--	--	--	--	--	--	--
Instrn[29]	--	--	--	--	--	--	--	--
Instrn[22]	--	--	--	--	--	--	--	--
Instrn[15]	--	--	--	--	--	--	--	--
Instrn[8]	--	--	--	--	--	--	--	--
Instrn[1]	--	--	--	--	--	--	--	--
Instrn[31]	--	--	--	--	--	--	--	--
Instrn[24]	--	--	--	--	--	--	--	--
Instrn[17]	--	--	--	--	--	--	--	--
Instrn[10]	--	--	--	--	--	--	--	--
Instrn[3]	--	--	--	--	--	--	--	--
Reset	--	--	--	--	--	--	--	--
Instrn[26]	--	--	--	--	--	--	--	--
Instrn[19]	--	--	--	--	--	--	--	--
Instrn[12]	--	--	--	--	--	--	--	--
Instrn[5]	--	--	--	--	--	--	--	--
Clk	--	--	--	--	--	--	--	--
Instrn[28]	--	--	--	--	--	--	--	--
Instrn[21]	--	--	--	--	--	--	--	--
Instrn[14]	--	--	--	--	--	--	--	--
Instrn[7]	--	--	--	--	--	--	--	--
Instrn[0]	--	--	--	--	--	--	--	--
Instrn[30]	--	--	--	--	--	--	--	--
Instrn[23]	--	--	--	--	--	--	--	--
Instrn[16]	--	--	--	--	--	--	--	--
Instrn[9]	--	--	--	--	--	--	--	--
Instrn[2]	--	--	--	--	--	--	--	--
Instrn[25]	--	--	--	--	--	--	--	--
Instrn[18]	--	--	--	--	--	--	--	--
Instrn[11]	--	--	--	--	--	--	--	--
Instrn[4]	--	--	--	--	--	--	--	--
Instrn[27]	--	--	--	--	--	--	--	--
Instrn[20]	--	--	--	--	--	--	--	--
Instrn[13]	--	--	--	--	--	--	--	--

Input Port	Max Tran		Min Tran	
	Rise	Fall	Rise	Fall

Instrn[6]	--	--	--	--
Instrn[29]	--	--	--	--
Instrn[22]	--	--	--	--
Instrn[15]	--	--	--	--
Instrn[8]	--	--	--	--
Instrn[1]	--	--	--	--
Instrn[31]	--	--	--	--
Instrn[24]	--	--	--	--
Instrn[17]	--	--	--	--
Instrn[10]	--	--	--	--
Instrn[3]	--	--	--	--
Reset	--	--	--	--
Instrn[26]	--	--	--	--
Instrn[19]	--	--	--	--
Instrn[12]	--	--	--	--

Instrn[5]	--	--	--	--
Clk	--	--	--	--
Instrn[28]	--	--	--	--
Instrn[21]	--	--	--	--
Instrn[14]	--	--	--	--
Instrn[7]	--	--	--	--
Instrn[0]	--	--	--	--
Instrn[30]	--	--	--	--
Instrn[23]	--	--	--	--
Instrn[16]	--	--	--	--
Instrn[9]	--	--	--	--
Instrn[2]	--	--	--	--
Instrn[25]	--	--	--	--
Instrn[18]	--	--	--	--
Instrn[11]	--	--	--	--
Instrn[4]	--	--	--	--
Instrn[27]	--	--	--	--
Instrn[20]	--	--	--	--
Instrn[13]	--	--	--	--

Output Port	Output Delay				Related Clock	Fanout Load
	Min Rise	Min Fall	Max Rise	Max Fall		

Xecutng_Instrn[2]	0.50	0.50	0.50	0.50	Clk	0.00
PSW[6]	0.50	0.50	0.50	0.50	Clk	0.00
PSW[9]	0.50	0.50	0.50	0.50	Clk	0.00
Xecutng_Instrn[25]	0.50	0.50	0.50	0.50	Clk	0.00
RESULT_DATA[11]	0.50	0.50	0.50	0.50	Clk	0.00
Xecutng_Instrn[18]	0.50	0.50	0.50	0.50	Clk	0.00
RESULT_DATA[4]	0.50	0.50	0.50	0.50	Clk	0.00
Xecutng_Instrn[11]	0.50	0.50	0.50	0.50	Clk	0.00
Xecutng_Instrn[4]	0.50	0.50	0.50	0.50	Clk	0.00
PSW[1]	0.50	0.50	0.50	0.50	Clk	0.00
Xecutng_Instrn[27]	0.50	0.50	0.50	0.50	Clk	0.00
RESULT_DATA[13]	0.50	0.50	0.50	0.50	Clk	0.00
Xecutng_Instrn[20]	0.50	0.50	0.50	0.50	Clk	0.00
RESULT_DATA[6]	0.50	0.50	0.50	0.50	Clk	0.00
Xecutng_Instrn[13]	0.50	0.50	0.50	0.50	Clk	0.00
Xecutng_Instrn[6]	0.50	0.50	0.50	0.50	Clk	0.00
PSW[3]	0.50	0.50	0.50	0.50	Clk	0.00
Xecutng_Instrn[29]	0.50	0.50	0.50	0.50	Clk	0.00
RESULT_DATA[15]						

	0.50	0.50	0.50	0.50	Clk	0.00
Xecutng_Instrn[22]	0.50	0.50	0.50	0.50	Clk	0.00
RESULT_DATA[8]	0.50	0.50	0.50	0.50	Clk	0.00
Xecutng_Instrn[15]	0.50	0.50	0.50	0.50	Clk	0.00
RESULT_DATA[1]	0.50	0.50	0.50	0.50	Clk	0.00
Xecutng_Instrn[8]	0.50	0.50	0.50	0.50	Clk	0.00
Xecutng_Instrn[1]	0.50	0.50	0.50	0.50	Clk	0.00
PSW[5]	0.50	0.50	0.50	0.50	Clk	0.00
PSW[8]	0.50	0.50	0.50	0.50	Clk	0.00
Xecutng_Instrn[31]	0.50	0.50	0.50	0.50	Clk	0.00
Rd_Instr	0.50	0.50	0.50	0.50	Clk	0.00
Xecutng_Instrn[24]	0.50	0.50	0.50	0.50	Clk	0.00
RESULT_DATA[10]	0.50	0.50	0.50	0.50	Clk	0.00
Xecutng_Instrn[17]	0.50	0.50	0.50	0.50	Clk	0.00
RESULT_DATA[3]	0.50	0.50	0.50	0.50	Clk	0.00
Xecutng_Instrn[10]	0.50	0.50	0.50	0.50	Clk	0.00
STACK_FULL	0.50	0.50	0.50	0.50	Clk	0.00
Xecutng_Instrn[3]	0.50	0.50	0.50	0.50	Clk	0.00
PSW[7]	0.50	0.50	0.50	0.50	Clk	0.00
PSW[10]	0.50	0.50	0.50	0.50	Clk	0.00
PSW[0]	0.50	0.50	0.50	0.50	Clk	0.00
Xecutng_Instrn[26]	0.50	0.50	0.50	0.50	Clk	0.00
RESULT_DATA[12]	0.50	0.50	0.50	0.50	Clk	0.00
Xecutng_Instrn[19]	0.50	0.50	0.50	0.50	Clk	0.00
RESULT_DATA[5]	0.50	0.50	0.50	0.50	Clk	0.00
Xecutng_Instrn[12]	0.50	0.50	0.50	0.50	Clk	0.00
OUT_VALID	0.50	0.50	0.50	0.50	Clk	0.00
Xecutng_Instrn[5]	0.50	0.50	0.50	0.50	Clk	0.00
EndOfInstrn	0.50	0.50	0.50	0.50	Clk	0.00
PSW[2]	0.50	0.50	0.50	0.50	Clk	0.00
Xecutng_Instrn[28]	0.50	0.50	0.50	0.50	Clk	0.00
RESULT_DATA[14]	0.50	0.50	0.50	0.50	Clk	0.00
Xecutng_Instrn[21]	0.50	0.50	0.50	0.50	Clk	0.00
RESULT_DATA[7]	0.50	0.50	0.50	0.50	Clk	0.00

Xecutng_Instrn[14]	0.50	0.50	0.50	0.50	Clk	0.00
RESULT_DATA[0]	0.50	0.50	0.50	0.50	Clk	0.00
Xecutng_Instrn[7]	0.50	0.50	0.50	0.50	Clk	0.00
Xecutng_Instrn[0]	0.50	0.50	0.50	0.50	Clk	0.00
PSW[4]	0.50	0.50	0.50	0.50	Clk	0.00
Xecutng_Instrn[30]	0.50	0.50	0.50	0.50	Clk	0.00
Xecutng_Instrn[23]	0.50	0.50	0.50	0.50	Clk	0.00
RESULT_DATA[9]	0.50	0.50	0.50	0.50	Clk	0.00
Xecutng_Instrn[16]	0.50	0.50	0.50	0.50	Clk	0.00
RESULT_DATA[2]	0.50	0.50	0.50	0.50	Clk	0.00
Xecutng_Instrn[9]	0.50	0.50	0.50	0.50	Clk	0.00

6. Report Cell

Report : cell

-connections

-verbose

Design : RISC_CORE

Version: 2003.06

Date : Mon Sep 13 13:39:59 2004

Connections for cell 'I_STACK_TOP/I2_STACK_MEM':

Reference: STACK_MEM_1

Hierarchical: TRUE

Area: 1952.87

dont_touch: FALSE

Input Pins	Net	Net Driver Pins	Driver Pin Type
------------	-----	-----------------	-----------------

-----	-----	-----	-----
Clk	I_STACK_TOP/Clk	Clk	Input Port

PushEnb1	I_STACK_TOP/PushEnb1	I_CONTROL/U129/Z	Output Pin
----------	----------------------	------------------	------------

(BUFM10P)

PopEnb1	I_STACK_TOP/PopEnb1	I_CONTROL/U132/Z	Output Pin
---------	---------------------	------------------	------------

(AND2M4P)

Stack_Full	I_STACK_TOP/STACK_FULL
------------	------------------------

I_STACK_TOP/I_STACK_FSM/STACK_FULL_reg/Q

(FD1LQM3P)			Output Pin
TOS[0]	I_STACK_TOP/TOS[0]		
I_STACK_TOP/I_STACK_FSM/TOS_int_reg[0]/Q			Output Pin
(FD1QM3P)			
TOS[1]	I_STACK_TOP/TOS[1]		
I_STACK_TOP/I_STACK_FSM/TOS_int_reg[1]/Q			Output Pin
(FD1QM3P)			
TOS[2]	I_STACK_TOP/TOS[2]		
I_STACK_TOP/I_STACK_FSM/TOS_int_reg[2]/Q			Output Pin
(FD1QM3P)			
PushDataIn[3]	I_STACK_TOP/PushDataIn[7]		
I_PRGRM_CNT_TOP/I_PRGRM_CNT/PCint_reg[7]/Q			Output Pin
(FD1LQM1P)			
PushDataIn[2]	I_STACK_TOP/PushDataIn[6]		
I_PRGRM_CNT_TOP/I_PRGRM_CNT/PCint_reg[6]/Q			Output Pin
(FD1LQM1P)			
PushDataIn[1]	I_STACK_TOP/PushDataIn[5]		
I_PRGRM_CNT_TOP/I_PRGRM_CNT/PCint_reg[5]/Q			Output Pin
(FD1LQM1P)			
PushDataIn[0]	I_STACK_TOP/PushDataIn[4]		
I_PRGRM_CNT_TOP/I_PRGRM_CNT/PCint_reg[4]/Q			Output Pin
(FD1LQM1P)			
Output Pins	Net	Net Load Pins	Load Pin Type
-----	-----	-----	-----
PopDataOut[3]	I_STACK_TOP/PopDataOut[7]		
I_PRGRM_CNT_TOP/I_PRGRM_CNT/U50/B			Input Pin
(A0222M2P)			
PopDataOut[2]	I_STACK_TOP/PopDataOut[6]		
I_PRGRM_CNT_TOP/I_PRGRM_CNT/U49/A			

(A0222M2P)	Input Pin
PopDataOut[1] I_STACK_TOP/PopDataOut[5]	
I_PRGRM_CNT_TOP/I_PRGRM_CNT/U48/A	
(A0222M2P)	Input Pin
PopDataOut[0] I_STACK_TOP/PopDataOut[4]	
I_PRGRM_CNT_TOP/I_PRGRM_CNT/U47/A	
(A0222M2P)	Input Pin

7. Report Net

Report : net

-min
-connections
-verbose

Design : RISC_CORE

Version: 2003.06

Date : Mon Sep 13 13:41:28 2004

net 'Oprnd_A[11]':

dont_touch: FALSE
pin capacitance: 0.0227
wire capacitance: 0.0323145
total capacitance: 0.0550145
wire resistance: 0.110102
number of drivers: 1
number of loads: 4
number of pins: 5

Connections for net 'Oprnd_A[11]':

Driver Pins	Type	Pin Cap

I_DATA_PATH/Oprnd_A_reg[11]/Q	Output Pin (FD1SLQM3P)	0

Load Pins	Type	Pin Cap

I_ALU/r355_11/U44/A	Input Pin (N1M1P)	0.0054
I_ALU/r355_11/U27/B	Input Pin (ND2BNM1P)	0.0032
I_ALU/U349/A	Input Pin (A022M1P)	0.0035
I_ALU/U397/S	Input Pin (MUX21HFM2P)	0.0106

net 'Oprnd_A[4]':

dont_touch: FALSE
pin capacitance: 0.0184
wire capacitance: 0.0323145
total capacitance: 0.0507145
wire resistance: 0.110102

number of drivers: 1
number of loads: 4
number of pins: 5

Connections for net 'Oprnd_A[4]':

Driver Pins	Type	Pin Cap
I_DATA_PATH/Oprnd_A_reg[4]/Q	Output Pin (FD1SLQM1P)	0
Load Pins	Type	Pin Cap
I_ALU/r355_11/U51/A	Input Pin (N1M1P)	0.0054
I_ALU/r355_11/U23/B	Input Pin (ND2BNM1P)	0.0032
I_ALU/U356/A	Input Pin (A022M1P)	0.0035
I_ALU/U248/S	Input Pin (MUX21HM1P)	0.0063

net 'Oprnd_A[13]':

dont_touch: FALSE
pin capacitance: 0.029
wire capacitance: 0.0323145
total capacitance: 0.0613145
wire resistance: 0.110102
number of drivers: 1
number of loads: 4
number of pins: 5

Connections for net 'Oprnd_A[13]':

Driver Pins	Type	Pin Cap
I_DATA_PATH/Oprnd_A_reg[13]/Q	Output Pin (FD1SLQM3P)	0
Load Pins	Type	Pin Cap
I_ALU/r355_11/U136/B	Input Pin (ND2BNM2P)	0.0043
I_ALU/r355_11/U100/A	Input Pin (N1M2P)	0.0106
I_ALU/U347/A	Input Pin (A022M1P)	0.0035
I_ALU/U393/S	Input Pin (MUX21HFM2P)	0.0106

net 'Oprnd_A[6]':

dont_touch: FALSE
pin capacitance: 0.0184
wire capacitance: 0.0323145
total capacitance: 0.0507145
wire resistance: 0.110102
number of drivers: 1
number of loads: 4
number of pins: 5

Connections for net 'Oprnd_A[6]':

Driver Pins	Type	Pin Cap
-------------	------	---------

```

I_DATA_PATH/Oprnd_A_reg[6]/Q
Output Pin (FD1SLQM1P)
0
Load Pins      Type      Pin Cap
-----
I_ALU/r355_11/U74/A Input Pin (N1M1P)  0.0054
I_ALU/r355_11/U16/B Input Pin (ND2BNM1P)
0.0032
I_ALU/U354/A      Input Pin (A022M1P) 0.0035
I_ALU/U234/S      Input Pin (MUX21HM1P)
0.0063
net 'Oprnd_A[15]':
dont_touch:      FALSE
pin capacitance:  0.0237
wire capacitance: 0.0229291
total capacitance: 0.0466291
wire resistance:  0.0781237
number of drivers: 1
number of loads:  3
number of pins:   4
Connections for net 'Oprnd_A[15]':

Driver Pins      Type      Pin Cap
-----
I_DATA_PATH/Oprnd_A_reg[15]/Q
Output Pin (FD1SLQM3P)
0
Load Pins      Type      Pin Cap
-----
I_ALU/r355_11/U103/A
Input Pin (E0FM2P) 0.0096
I_ALU/U345/A      Input Pin (A022M1P) 0.0035
I_ALU/U381/S      Input Pin (MUX21HFM2P)
0.0106
net 'Oprnd_A[8]':
dont_touch:      FALSE
pin capacitance:  0.0184
wire capacitance: 0.0323145
total capacitance: 0.0507145
wire resistance:  0.110102
number of drivers: 1
number of loads:  4
number of pins:   5
Connections for net 'Oprnd_A[8]':

Driver Pins      Type      Pin Cap
-----
I_DATA_PATH/Oprnd_A_reg[8]/Q
Output Pin (FD1SLQM1P)
0
Load Pins      Type      Pin Cap
-----
I_ALU/r355_11/U71/A Input Pin (N1M1P)  0.0054
I_ALU/r355_11/U22/B Input Pin (ND2BNM1P)
0.0032
I_ALU/U352/A      Input Pin (A022M1P) 0.0035
I_ALU/U241/S      Input Pin (MUX21HM1P)

```

```

0.0063
net 'Oprnd_A[1]':
  dont_touch:      FALSE
  pin capacitance:  0.0184
  wire capacitance: 0.0323145
  total capacitance: 0.0507145
  wire resistance:  0.110102
  number of drivers: 1
  number of loads:  4
  number of pins:   5
Connections for net 'Oprnd_A[1]':

  Driver Pins      Type      Pin Cap
  -----
  I_DATA_PATH/Oprnd_A_reg[1]/Q
                        Output Pin (FD1SLQM3P)
                        0
  Load Pins      Type      Pin Cap
  -----
  I_ALU/r355_11/U60/B Input Pin (ND2BNM1P)
                        0.0032
  I_ALU/r355_11/U63/A Input Pin (N1M1P)   0.0054
  I_ALU/U359/A       Input Pin (A022M1P) 0.0035
  I_ALU/U311/S       Input Pin (MUX21HM1P)
                        0.0063

net 'Oprnd_A[10]':
  dont_touch:      FALSE
  pin capacitance:  0.0227
  wire capacitance: 0.0323145
  total capacitance: 0.0550145
  wire resistance:  0.110102
  number of drivers: 1
  number of loads:  4
  number of pins:   5
Connections for net 'Oprnd_A[10]':

  Driver Pins      Type      Pin Cap
  -----
  I_DATA_PATH/Oprnd_A_reg[10]/Q
                        Output Pin (FD1SLQM3P)
                        0
  Load Pins      Type      Pin Cap
  -----
  I_ALU/r355_11/U34/B Input Pin (ND2BNM1P)
                        0.0032
  I_ALU/r355_11/U36/A Input Pin (N1M1P)   0.0054
  I_ALU/U350/A       Input Pin (A022M1P) 0.0035
  I_ALU/U398/S       Input Pin (MUX21HFM2P)
                        0.0106

net 'Oprnd_A[3]':
  dont_touch:      FALSE
  pin capacitance:  0.0184
  wire capacitance: 0.0323145
  total capacitance: 0.0507145
  wire resistance:  0.110102
  number of drivers: 1
  number of loads:  4

```

number of pins: 5
Connections for net 'Oprnd_A[3]':

Driver Pins	Type	Pin Cap
I_DATA_PATH/Oprnd_A_reg[3]/Q	Output Pin (FD1SLQM1P)	0
Load Pins	Type	Pin Cap
I_ALU/r355_11/U65/B	Input Pin (ND2BNM1P)	0.0032
I_ALU/r355_11/U67/A	Input Pin (N1M1P)	0.0054
I_ALU/U357/A	Input Pin (A022M1P)	0.0035
I_ALU/U274/S	Input Pin (MUX21HM1P)	0.0063

net 'Oprnd_A[12]':
dont_touch: FALSE
pin capacitance: 0.0227
wire capacitance: 0.0323145
total capacitance: 0.0550145
wire resistance: 0.110102
number of drivers: 1
number of loads: 4
number of pins: 5
Connections for net 'Oprnd_A[12]':

Driver Pins	Type	Pin Cap
I_DATA_PATH/Oprnd_A_reg[12]/Q	Output Pin (FD1SLQM1P)	0
Load Pins	Type	Pin Cap
I_ALU/r355_11/U75/A	Input Pin (N1M1P)	0.0054
I_ALU/r355_11/U42/B	Input Pin (ND2BNM1P)	0.0032
I_ALU/U348/A	Input Pin (A022M1P)	0.0035
I_ALU/U396/S	Input Pin (MUX21HFM2P)	0.0106

net 'Oprnd_A[5]':
dont_touch: FALSE
pin capacitance: 0.0184
wire capacitance: 0.0323145
total capacitance: 0.0507145
wire resistance: 0.110102
number of drivers: 1
number of loads: 4
number of pins: 5
Connections for net 'Oprnd_A[5]':

Driver Pins	Type	Pin Cap
I_DATA_PATH/Oprnd_A_reg[5]/Q	Output Pin (FD1SLQM1P)	0
Load Pins	Type	Pin Cap

```

-----
I_ALU/r355_11/U76/A Input Pin (N1M1P) 0.0054
I_ALU/r355_11/U14/B Input Pin (ND2BNM1P)
                                0.0032
I_ALU/U355/A          Input Pin (A022M1P) 0.0035
I_ALU/U281/S          Input Pin (MUX21HM1P)
                                0.0063
net 'Oprnd_A[14]':
dont_touch:          FALSE
pin capacitance:     0.0238
wire capacitance:    0.0323145
total capacitance:   0.0561145
wire resistance:     0.110102
number of drivers:    1
number of loads:      4
number of pins:       5
Connections for net 'Oprnd_A[14]':

Driver Pins          Type          Pin Cap
-----
I_DATA_PATH/Oprnd_A_reg[14]/Q
                        Output Pin (FD1SLQM1P)
                        0
Load Pins            Type          Pin Cap
-----
I_ALU/r355_11/U73/A Input Pin (N1M1P) 0.0054
I_ALU/r355_11/U140/B Input Pin (ND2BNM2P)
                                0.0043
I_ALU/U346/A          Input Pin (A022M1P) 0.0035
I_ALU/U388/S          Input Pin (MUX21HFM2P)
                                0.0106
net 'Oprnd_A[7]':
dont_touch:          FALSE
pin capacitance:     0.0184
wire capacitance:    0.0323145
total capacitance:   0.0507145
wire resistance:     0.110102
number of drivers:    1
number of loads:      4
number of pins:       5
Connections for net 'Oprnd_A[7]':

Driver Pins          Type          Pin Cap
-----
I_DATA_PATH/Oprnd_A_reg[7]/Q
                        Output Pin (FD1SLQM1P)
                        0
Load Pins            Type          Pin Cap
-----
I_ALU/r355_11/U72/A Input Pin (N1M1P) 0.0054
I_ALU/r355_11/U19/B Input Pin (ND2BNM1P)
                                0.0032
I_ALU/U353/A          Input Pin (A022M1P) 0.0035
I_ALU/U245/S          Input Pin (MUX21HM1P)
                                0.0063
net 'Oprnd_A[0]':

```

dont_touch: FALSE
pin capacitance: 0.0152
wire capacitance: 0.0229291
total capacitance: 0.0381291
wire resistance: 0.0781237
number of drivers: 1
number of loads: 3
number of pins: 4

Connections for net 'Oprnd_A[0]':

Driver Pins	Type	Pin Cap
I_DATA_PATH/Oprnd_A_reg[0]/Q	Output Pin (FD1SLQM1P)	0
Load Pins	Type	Pin Cap
I_ALU/r355_11/U29/A	Input Pin (N1M1P)	0.0054
I_ALU/U360/A	Input Pin (A022M1P)	0.0035
I_ALU/U309/S	Input Pin (MUX21HM1P)	0.0063

net 'Oprnd_A[9]':

dont_touch: FALSE
pin capacitance: 0.0184
wire capacitance: 0.0323145
total capacitance: 0.0507145
wire resistance: 0.110102
number of drivers: 1
number of loads: 4
number of pins: 5

Connections for net 'Oprnd_A[9]':

Driver Pins	Type	Pin Cap
I_DATA_PATH/Oprnd_A_reg[9]/Q	Output Pin (FD1SLQM1P)	0
Load Pins	Type	Pin Cap
I_ALU/r355_11/U53/A	Input Pin (N1M1P)	0.0054
I_ALU/r355_11/U38/B	Input Pin (ND2BNM1P)	0.0032
I_ALU/U351/A	Input Pin (A022M1P)	0.0035
I_ALU/U257/S	Input Pin (MUX21HM1P)	0.0063

net 'Oprnd_A[2]':

dont_touch: FALSE
pin capacitance: 0.0195
wire capacitance: 0.0323145
total capacitance: 0.0518145
wire resistance: 0.110102
number of drivers: 1
number of loads: 4
number of pins: 5

Connections for net 'Oprnd_A[2]':

Driver Pins	Type	Pin Cap
-------------	------	---------

```

-----
I_DATA_PATH/Oprnd_A_reg[2]/Q
                                Output Pin (FD1SLQM3P)
                                0
Load Pins                      Type                      Pin Cap
-----
I_ALU/r355_11/U110/B
                                Input Pin (ND2BNM2P)
                                0.0043
I_ALU/r355_11/U58/A Input Pin (N1M1P) 0.0054
I_ALU/U358/A      Input Pin (A022M1P) 0.0035
I_ALU/U314/S      Input Pin (MUX21HM1P)
                                0.0063

```

8. Report Clock

```

*****
Report : clocks
Design : RISC_CORE
Version: 2003.06
Date   : Mon Sep 13 13:42:39 2004
*****

```

Attributes:

```

d - dont_touch_network
f - fix_hold
p - propagated_clock
G - generated_clock

```

Clock	Period	Waveform	Attrs	Sources
Clk	4.00	{0 2}		{Clk}

9. Report Area

```

*****
Report : area
Design : RISC_CORE
Version: 2003.06
Date   : Mon Sep 13 13:43:16 2004
*****

```

Library(s) Used:

```

gflxp (File:
/usr/apps/eda/flexstream.3.3/lsi_fs_3.3/lib3p/synopsys/gflxp/gflxp_lsi_
wc.db)

```

```

Number of ports:          97
Number of nets:           278
Number of cells:          41
Number of references:      9
Combinational area:       9271.859375
Noncombinational area:    9372.499023
Net Interconnect area:    8347.217773
Total cell area:          18644.380859
Total area:                26991.578125

```

10. Report Compile Options

Report : compile_options

Design : RISC_CORE

Version: 2003.06

Date : Mon Sep 13 13:44:51 2004

Design	Compile Option	Value

RISC_CORE	flatten	false
	structure	true
	structure_boolean	false
	structure_timing	true
	isolate_port	
disabled ALU	flatten	false
	structure	true
	structure_boolean	false
	structure_timing	true
ALU_DW01_addsub_16_2	flatten	false
	structure	true
	structure_boolean	false
	structure_timing	true
ALU_DW01_addsub_16_0	flatten	false
	structure	true
	structure_boolean	false
	structure_timing	true
CONTROL	flatten	false
	structure	true
	structure_boolean	false
	structure_timing	true
DATA_PATH	flatten	false
	structure	true
	structure_boolean	false
	structure_timing	true
INSTRN_LAT	flatten	false
	structure	true
	structure_boolean	false
	structure_timing	true
PRGRM_CNT_TOP	flatten	false
	structure	true
	structure_boolean	false
	structure_timing	true
PRGRM_FSM	flatten	false
	structure	true
	structure_boolean	false
	structure_timing	true
PRGRM_DECODE	flatten	false
	structure	true
	structure_boolean	false
	structure_timing	true
PRGRM_CNT	flatten	false
	structure	true

PRGRM_CNT_DW01_inc_8_0	structure_boolean	false
	structure_timing	true
	flatten	false
	structure	true
	structure_boolean	false
REG_FILE	structure_timing	true
	flatten	false
	structure	true
	structure_boolean	false
STACK_TOP	structure_timing	true
	flatten	false
	structure	true
	structure_boolean	false
STACK_FSM	structure_timing	true
	flatten	false
	structure	true
	structure_boolean	false
STACK_MEM_2	structure_timing	true
	flatten	false
	structure	true
	structure_boolean	false
STACK_MEM_1	structure_timing	true
	flatten	false
	structure	true
	structure_boolean	false
STACK_MEM_0	structure_timing	true
	flatten	false
	structure	true
	structure_boolean	false
	structure_timing	true

11. Report Power

Report : power
 -analysis_effort low
 -verbose

Design : RISC_CORE

Version: 2003.06

Date : Mon Sep 13 13:46:15 2004

Library(s) Used:

gflxp (File:
 /usr/apps/eda/flexstream.3.3/lsi_fs_3.3/lib3p/synopsys/gflxp/gflxp_lsi_
 wc.db)
 Operating Conditions: LSI_WC Library: gflxp
 Wire Load Model Mode: enclosed

Design	Wire Load Model	Library

RISC_CORE	B1X1	gflxp
ALU	B0.2X0.2	gflxp
ALU_DW01_addsub_16_2	B0.1X0.1	gflxp
ALU_DW01_addsub_16_0	B0.1X0.1	gflxp
CONTROL	B0.1X0.1	gflxp
DATA_PATH	B0.1X0.1	gflxp
INSTRN_LAT	B0.1X0.1	gflxp
PRGRM_CNT_TOP	B0.1X0.1	gflxp
PRGRM_FSM	B0.1X0.1	gflxp
PRGRM_DECODE	B0.1X0.1	gflxp
PRGRM_CNT	B0.1X0.1	gflxp
PRGRM_CNT_DW01_inc_8_0	B0.1X0.1	gflxp
REG_FILE	B0.2X0.2	gflxp
STACK_TOP	B0.2X0.2	gflxp
STACK_FSM	B0.1X0.1	gflxp
STACK_MEM_2	B0.1X0.1	gflxp
STACK_MEM_1	B0.1X0.1	gflxp
STACK_MEM_0	B0.1X0.1	gflxp

Global Operating Voltage = 1.08
Power-specific unit information :
Voltage Units = 1V
Capacitance Units = 1.000000pf
Time Units = 1ns
Dynamic Power Units = 1mW (derived from V,C,T units)
Leakage Power Units = Unitless
Cell Internal Power Breakdown

Combinational	= 329.1682 uW	(4%)
Sequential	= 5.4080 mW	(73%)
Other	= 0.0000 mW	(0%)
Combinational Count	= 1298	
Sequential Count	= 310	
Other Count	= 0	
Cell Internal Power	= 5.7371 mW	(77%)
Net Switching Power	= 1.7060 mW	(23%)

Total Dynamic Power	= 7.4432 mW	(100%)
Cell Leakage Power	= 0.0000	